域格信息技术有限公司

YuGe Information Technology Co.,Ltd

CLM920_TD5 LTE Module Hardware Manual

Version 1.1

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1 Introduction

This document is the hardware interface manual of the wireless solution product CLM920_TD5 Mini PCIE module. It is intended to describe the hardware composition and functional characteristics of the module solution product, application interface definition and usage, electrical and mechanical characteristics, etc., provide hardware instructions for users' application development based on the product.

2 Product Overview

2.1 General Description

CLM920_TD5 Mini PCIE module provides data connectivity on FDD / TDD / TD-SCDMA / UMTS / EVDO / CDMA / EDGE / GSM networks and inergrated GPS service with PCI Express Mini Card 1.2 standard interface. The module bases on Qualcomm's MDM9X07, supports Cat4 which upload/download speed can reach 50Mbps/150Mbps, fully supports VOLTE and SRLTE and supports emdedded operating system such as Windows 7/Windows 8/Windows 10/Android /Linux/WinCE.

CLM920_TD5 module can be applied in the following applications:

- ✧ Vehicle System
- ✧ Wireless POS System
- ✧ Wireless Advertising, media
- ✧ Remote Monitor System
- ✧ Intelligent Meter Reading System
- ✧ Mobile Broadband
- ✧ Industrial Automation
- ✧ Other Wireless Terminal Device

2.2 Key Features

Table 2- 1 Operating frequency band

Network	Band	Product Series
		CLM920_TD5
GSM	GSM850	●
	GSM900	●
	GSM1800	●

	GSM1900	●
LTE(FDD)	LTE FDD B1	●
	LTE FDD B2	●
	LTE FDD B3	●
	LTE FDD B4	●
	LTE FDD B5	●
	LTE FDD B7	●
	LTE FDD B8	●
	LTE FDD B17	●
	LTE FDD B20	●
	LTE FDD B28	●
LTE(TDD)	LTE TDD B38	●
	LTE TDD B39	●
	LTE TDD B40	●
	LTE TDD B41	●
TD-SCDMA	TD-SCDMA B34	●
	TD-SCDMA B39	●
WCDMA	BAND 1	●
	BAND 2	●
	BAND 5	●
	BAND 8	●
CDMA2000/EVDO	BC0	optional
GNSS	GLONASS	●
	GPS	●
	BeiDou/Compass	●
Category 1		●

NOTE

① GNSS function is optional.

② The module supports Category 4 as default. The module label will notes CAT 1 when it supports Category 1. CAT1 doesn’t support diversity.

Table 2- 2 Key Features

Feature	Details
Physical Characteristics	51mmx30mmx4.1mm
Mounting	Grounding screw holes (2)
Application processor	Single-core ARM Cortex-A7 processor, clocked at 1.2GHZ, 256kB level 2 cache
Power Supply	3.3V - 4.2V Typical supply voltage:3.7V

Standby Current	< 5mA
Application Interface	✧ Standard SIM interface, support 3.0V/1.8V, support hot plug ✧ USB2.0 (High-Speed) ✧ Hardware reset interface ✧ UART serial interface ✧ PCM/Analog voice interface ✧ Power interface ✧ Network status indication interface ✧ GPIO interface
Antenna connector	Main Antenna Connector (MM4829-2702RA4) Diversity Antenna connectorMM4829-2702RA4) GPS Antenna connector (MM4829-2702RA4)
Transmitting Power	LTE: Class 3 (23dBm±2dB) UMTS: Class 3 (24dBm+1/-3dB) TD-SCDMA: Class 2 (24dBm+1/-3dB) CDMA2000: Class 3 (24dBm+3/-1dB) GSM/GPRS: Class 4 (33dBm±2dB) GSM850/GSM900 Class 1 (30dBm±2dB) DCS1800/PCS1900
Data services	GSM/EDGE: ✧ GPRS: DL 85.6 kbps/UL 85.6 kbps ✧ EDGE: DL 236.8 kbps/UL 236.8 kbps WCDMA: ✧ UMTS R99: DL 384 kbps/UL 384 kbps ✧ DC-HSPA+: DL 42 Mbps/UL 5.76 Mbps TD-SCDMA: ✧ TD-HSDPA/HSUPA: 2.2Mbps (UL) /2.8Mbps (DL) EV-DOr0/DOrA ✧ CDMA 1xEVDOr0: DL 2.4Mbps/UL 153kbps ✧ CDMA 1xEVDOrA: DL 3.1Mbps/UL 1.8Mbps LTE: ✧ LTE FDD:DL 150Mbps/UL 50Mbps@20M BW cat4 ✧ LTE TDD:DL 130Mbps/UL 35Mbps@20M BW cat4 ✧ LTE FDD:DL 10Mbps/UL 5Mbps@20M BW cat1 ✧ LTE TDD:DL 10Mbps/UL 5Mbps@20M BW cat1
Satellite	GPS/BEIDOU/GLONASS

positioning	Protocol: NMEA
Diversity antenna	Supports LTE diversity antenna
AT instruction	Supports standard AT command set (Hayes 3GPP TS 27.007 和 27.005)
SMS	Text and PDU mode Point to point MO and MT SMS storage: USIM card/ME by default
Virtual network card	Support USB virtual network card
Temperature Range	✧ Normal operation: -35° C to +75° C ✧ Restricted operation: -40° C to +85° C ✧ Storage temperature: -45° C to +90° C
Module function distinction	On the label paper M shorts for the main set, D shorts for diversity, G shorts for GPS, V shorts for analog voice

2.3 Module Function

CLM920_TD5 Mini PCIE module contains the following circuit elements:

- ✧ Baseband processing unit
- ✧ Power management unit
- ✧ Memory unit
- ✧ RF transceiver unit
- ✧ RF front-end unit
- ✧ GPS RF receiving unit

CLM920_TD5 Mini PCIE module function block diagram is as follows:

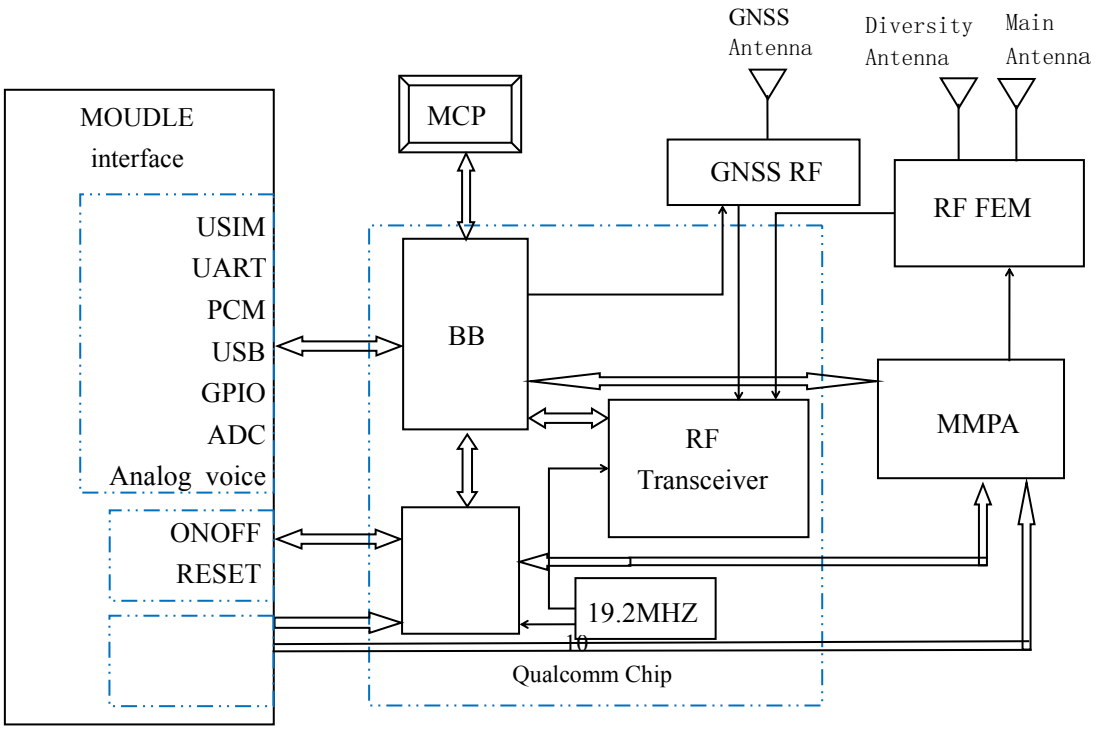

Figure 2- 1 CLM920_TD5 Mini PCIE Functional Diagram

3 Application Interface

3.1 General Description

This chapter mainly describes the application interface of this module. Contains the following sections:

- ✧ 52-pin Goldfinger
- ✧ Interface definition
- ✧ Power interface
- ✧ USB interface
- ✧ USIM interface
- ✧ UART interface
- ✧ WWAN control interface
- ✧ PCM/Analog voice interface
- ✧ RF antenna interface

3.2 Module Interface

3.2.1 52-pin Goldfinger

The CLM920_TD5 Mini PCIE module using 52-pin Mini PCIE Goldfinger as an external interactive interface.

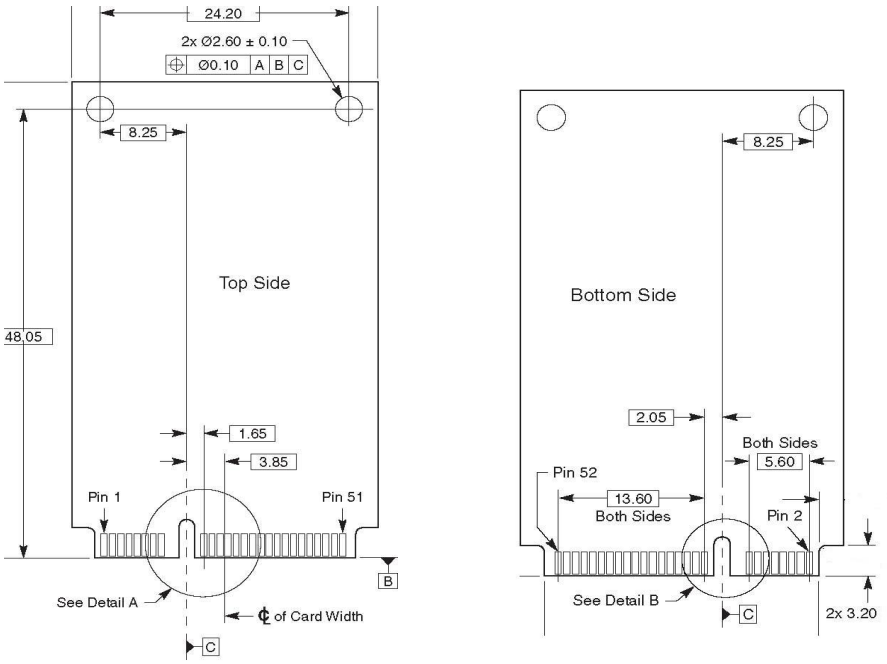

Figure 3- 1 TOP and BOTTOM of Goldfinger

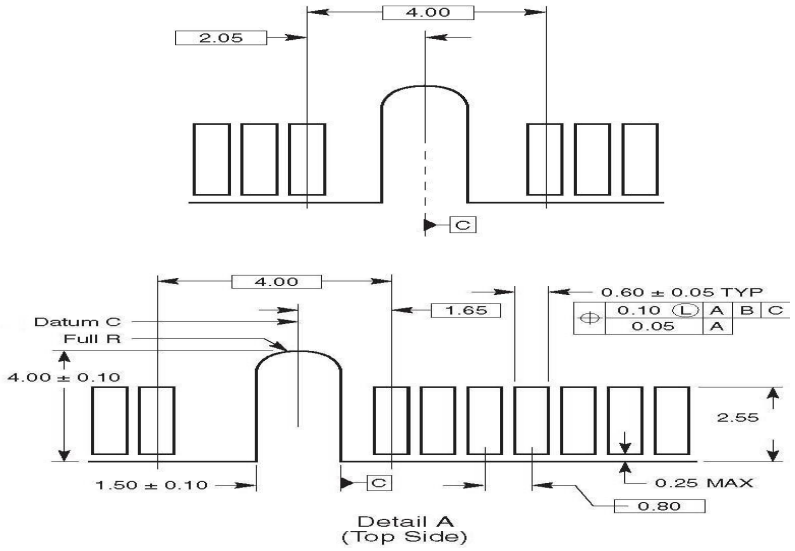

Figure 3- 2 TOP and BOTTOM of Goldfinger Detail A&B

3.2.2 Interface definition

CLM920_TD5 Mini PCIE module interface is the standard Mini PCI Express interface. The interface definition of the module is as below:

Table 3- 1 IO parameter definitions

Symbol	Description
IO	Bidirectional input and output

PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
DI	Digital input
DO	Digital output

Table 3- 2 Interface definitions

Pin	Standard Pin Definitions	Module pin definition	IO	Functional description	Remarks
1	WAKE#	MIC+	AI	Audio input+	
2	3.3Vaux	VBAT	PI	Power input	
3	COEX1	MIC-	AI	Audio Input-	
4	GND	GND		Ground	
5	COEX2	SPK+/REC+	AO	Audio output+	set headset or speaker by AT
6	1.5V	UIM_DET	DI	SIM hot plug detection	
7	CLKREQ#	SPK-/REC-	AO	Audio output-	set headset or speaker by AT
8	UIM_PWR	UIM_PWR	PO	SIM power supply	
9	GND	GND		Ground	
10	UIM_DATA	UIM_DATA	IO	SIM card data signal	
11	REFCLK-	UART_RX	DI	Serial receive	
12	UIM_CLK	UIM_CLK	DO	SIM card clock signal	
13	REFCLK+	UART_TX	DO	Serial transmission	
14	UIM_RESET	UIM_RESET	DO	SIM reset signal	
15	GND	GND		Ground	
16	UIM_VPP	NC			
17	RESERVED	VDD_EXT	PO	1.8V output	
18	GND	GND		Ground	
19	RESERVED	WAKEUP_IN	DI	HOST wake up module	1.8V, Active low

20	W_DISABLE#	W_DISABLE#	DI	turn off RF	Active low
21	GND	GND		Ground	
22	PERST#	RESET	DI	Reset control	Active low
23	PERn0	UART_CTS	DI	Serial Port Send Clear	
24	3.3Vaux	VBAT	PI	power input	
25	PERp0	UART_RTS	DO	Serial request to send	
26	GND	GND		Ground	
27	GND	GND		Ground	
28	1.5V	NC			
29	GND	GND		Ground	
30	SMB_CLK	NC			
31	PETn0	NC			
32	SMB_DATA	WAKEUP_OUT	DO	module wakes up the HOST	
33	PETp0	NC			
34	GND	GND		Ground	
35	GND	GND		Ground	
36	USB_D-	USB_DM	IO	USB Differential Signals -	
37	GND	GND		Ground	
38	USB_D+	USB_DP	IO	USB Differential Signals +	
39	3.3Vaux	VBAT	PI	Power input	
40	GND	GND		Ground	
41	3.3Vaux	VBAT	PI	Power input	
42	LED_WWAN#	LED_WWAN#	OC	Status light indication	
43	GND	GND		Ground	
44	LED_WLAN#	UIM_DET	DI	SIM hot plug detection	Reserved
45	RESERVED	PCM_CLK	DO	PCM clock pulse	
46	LED_WPAN#	NC			Reserved
47	RESERVED	PCM_DOUT	DO	PCM data output	

48	1.5V	NC		
49	RESERVED	PCM_DIN	DI	PCM data input
50	GND	GND		Ground
51	RESERVED	PCM_SYNC	DO	PCM frame sync
52	3.3Vaux	VBAT	PI	Power input

NOTE

① The module's general IO port level is 1.8V (except SIM, the SIM card port level supports 1.8V and 3.0V).
② Shall not use the module's pins which are defined as RESERVED or NC, they need to be floated.

3.3 Power Interface

CLM920_TD5 Mini PCIE module power interface consists of two parts:

- VBAT for the module power supply;
- UIM_PWR for SIM card operation power supply;
- VDD_EXT for 1.8V output supply;

3.3.1 Power Design

CLM920_TD5 Mini PCIE module power interface is as follows:

Table 3- 3 Power pin definitions

Pin	Name	I/O	Description	Min voltage	Typical voltage	Max voltage
2,24,39,41,52	VBAT	PI	Module power supply	3.4V	3.7V	4.2V
8	UIM_PWR	PO	SIM power supply	0	1.8V/2.85V	1.9/2.95V
17	VDD_EXT	PO	Output power		1.8V	
4,9,15,18,21,26,27,29,34,35,37,40,43,50	GND		Ground	-	0	-

CLM920_TD5 Mini PCIE module with single power supply mode, the module provides 5-way power supply pin, 14-way pin. VBAT power supply range of 3.3-4.2V, the proposed power supply is 3.7V / 2A . The module's peak current will reach 2.5A when transmit data or call under HSPA/UTMS/GSM, which resulting in a large ripple on the power. If instant voltage drop makes the VBAT power too low or the current supply

insufficient, the module will power off or restart. To ensure that the module works, all power and ground pins should be connected to use and able to prvide enough power supply.

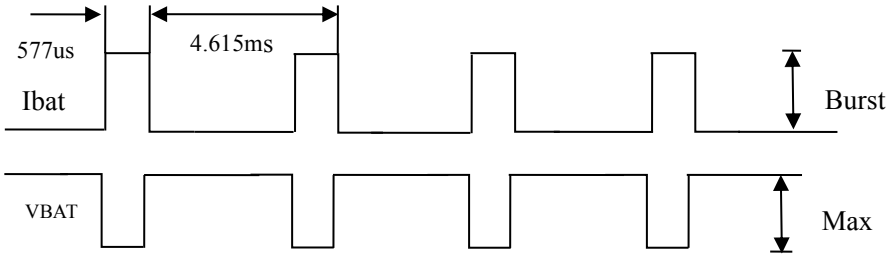

Figure 3- 3 GSM TDMA Power Supply Voltage Drop

On the premise of the VBAT can provide enough power, connect two 470uF/6.3V tantalum capacitors in parallel near to the power, also connect another 10pF, 33pF, 0.1uF, 1uF ceramic capacitors.

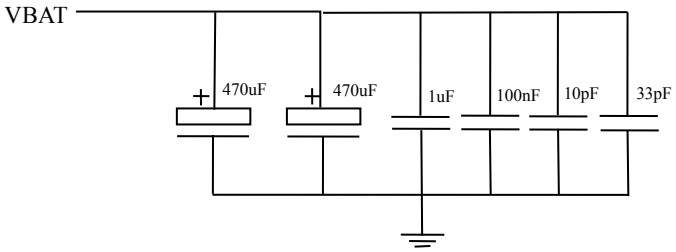

Figure 3- 4 VBAT Power Supply

3.3.2 Reference Design of Power Supply

Actual design can use DC switching power supply or LDO linear power supply, both design circuit needs to provide enough current. Refer to the following design:

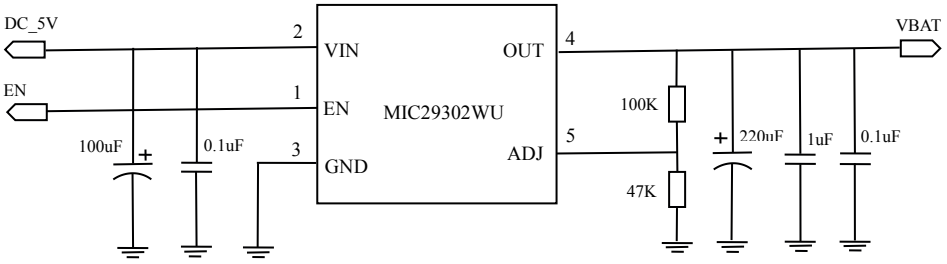

Figure 3- 5 Reference Design of LDO linear power supply

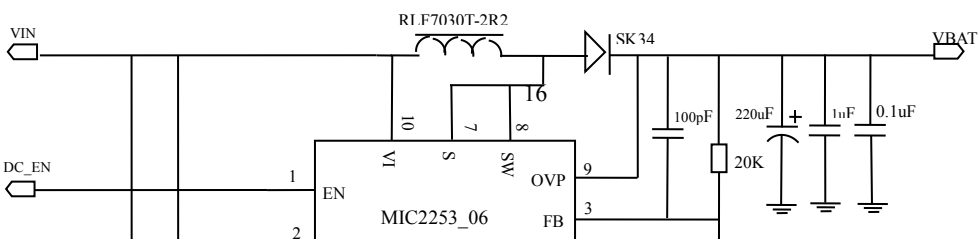

Figure 3- 6 Reference Design of DC switching power supply

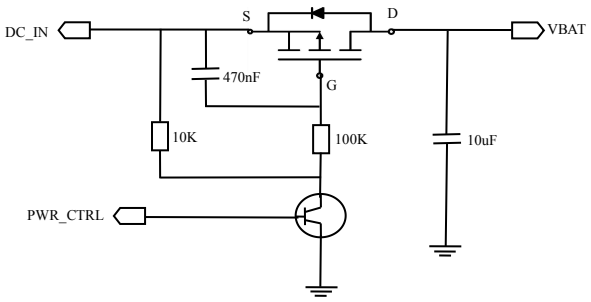

Figure 3- 7 Reference Design of PMOS tube to control the power switch

NOTE

① In order to prevent the surge and overvoltage damage the module, suggest that connect a 5.1 V / 500 mw zener diodeon to the module's VBAT pin in parallel.

② Suggest that use another three ceramic capacitors (33pF ,10pF,100nF) near to the VBAT pin.

③ The minimum working voltage of the module is 3.3V. Due to the peak current will reach 2.5A when transmit data or call under GSM making a large ripple on the power, the supply voltage can't lower than 3.3V.

3.3.3 VDD_EXT 1V8 output

The pin 17 will output 1.8V after CLM920_TD5 Mini PCIE module boots up normally. Its maximum current load is 50mA. The external master can determine whether the module works by reading the voltage of the VDD_EXT. The VDD_EXT can also be used as external power supply, such as level conversion chip, etc.

3.4 Reset mode

CLM920_TD5 Mini PCIE module will work after be gived the correct power supply. Users can determine whether the module works by reading the voltage of the VDD_EXT.

Table 3- 4 Reset Pin Definition

Pin	Name	I/O	High value	Description
22	RESET	DI	1.8V	Module reset control pin, active low
28	PWRKEY	NC	NC	NC

3.4.1 Power-on sequence

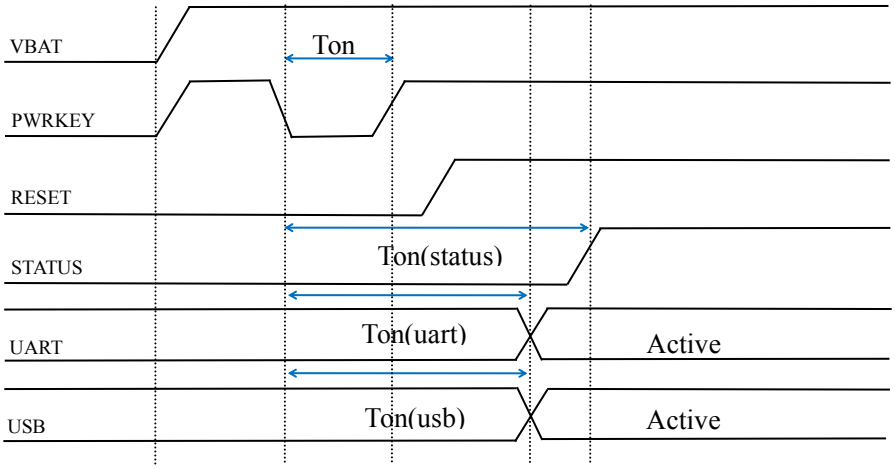

Figure 3- 8 Power-on sequence diagram

Table 3- 5 Power-on sequence parameters

Symbol	Description	Min	Typical	Max	Unit
Ton	Low level width of boot	100	500	-	ms
Ton(status)	Boot time(Judge by the status)	22	-	-	ms
Ton(usb)	Boot time(Judge by the USB)	-	20	-	ms
Ton(uart)	Boot time(Judge by the UART)	-	20	-	ms
VIH	PWRKEY high level input	0.6	0.8	1.8	V
VIL	PWRKEY low level input	-0.3	0	0.5	V

3.4.2 Power off

The module without a normal shutdown process when turn it off by cutting off the VBAT power supply. Only if the module is abnormal and can’t restart by AT, cutting off the VBAT power supply can be used。

3.4.3 Reset control

CLM920_TD5 Mini PCIE module’s reset pin is 22. Pull this pin low 150-450 ms to

reset the module. This pin is sensitive to interference ratio, the alignment should pay attention to protection.

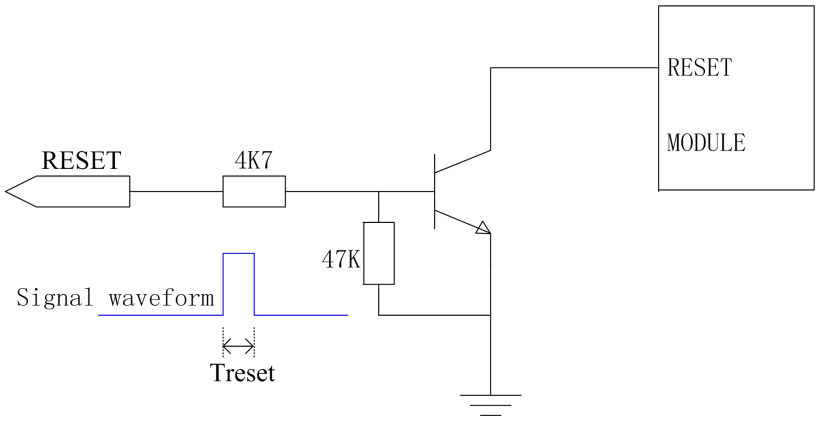

Figure 3- 9 Reset Reference Circuit

Table 3- 6 RESET Pin Definitions

Symbol	Description	Min	Typical	Max	Unit
Treset	Low level pulse width	150	200	450	ms
VIH	RESET high level input	1.17	1.8	2.1	V
VIL	RESET low level input	-0.3	0	0.8	V

RESET sequence:

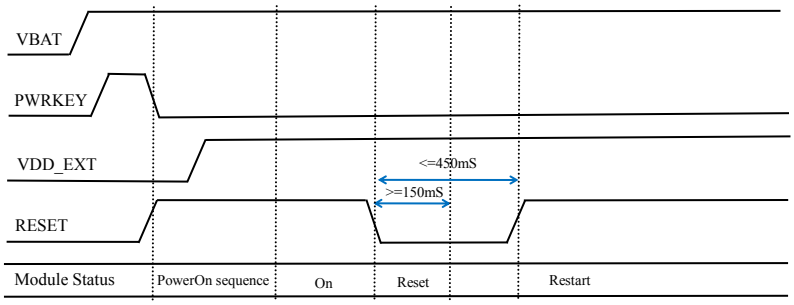

Figure 3- 10 RESET sequence diagram

CLM920_TD5 Mini PCIE module support used AT command to reset, the AT command is AT+CFUN=1,1. Detials can check the CLM920_TD5 AT command manual.

3.5 USB interface

CLM920_TD5 Mini PCIE module's USB interface supports USB2.0 high-speed protocol. Interface supports pattern from the device, does not support USB charging mode. USB interface is defined as follows:

Table 3- 7 USB interface pin definitions

Pin	Signal name	IO	Description
36	USB_DM	IO	USB differential signal -
38	USB_DP	IO	USB differential signal +
4, 9, 15, 18, 21, 26, 27, 29, 34, 35, 37, 40, 43, 50	GND		Ground

Module as a USB device, support USB mechanism of sleep and wake up. The USB reference design circuit is as follows:

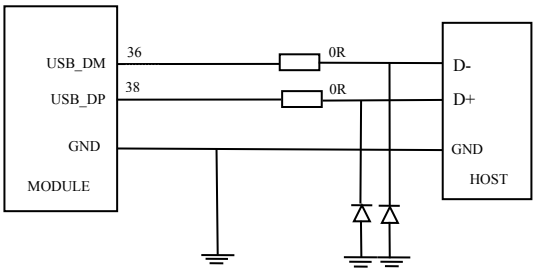

Figure 3- 11 USB design circuit diagram

NOTE

① USB interface supports High speed(480Mbps) and Full speed(12Mbps) mode. USB traces designed to strictly follow the USB2.0 protocol requirements, wiring attention to the data line protection, differential traces, the control impedance of 90Ω.

② In order to improve the antistatic performance of USB interface, it is recommended that ESD protection devices should be added to the data lines, the equivalent capacitance of protection device less than 2pF.

③ USB bus power supply voltage provided by the module, without external provision. Meanwhile, the module can only be used as the slave device of the USB bus, because the module's USB interface does not provide external USB bus power.

USB interface supports the following functions:

- ✧ Software download and upgrade
- ✧ Data communication
- ✧ AT Command
- ✧ GNSS NMEA output

3.6 UART interface

CLM920_TD5 Mini PCIE module provides a set of UART interface, the level is 1.8V. This interface can be used for AT communication and printing program log information.

The UART interface supports 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800

and 921600bps baud rate. The default is 115200bps.

UART interface is defined as follows:

Table 3- 8 UARTserial signal definitions

Pin	Signal name	I/O	Description
11	UART_RX	DI	UART receive data
13	UART_TX	DO	UART transmit data
23	UART_CTS	DI	user allows the module to transmit
25	UART_RTS	DO	Module requests the user to send

If need to use the serial port, please refer to the following serial port design.

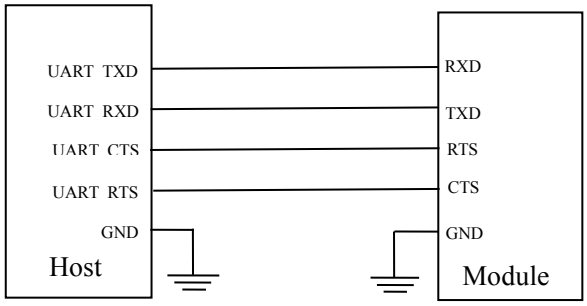

Figure 3- 12 UART serial port design

The module's UART port level is 1.8V. A level conversion chip is needed when connect the port to the MCU whose level is 3.3V. The connection can refer to the following circuit:

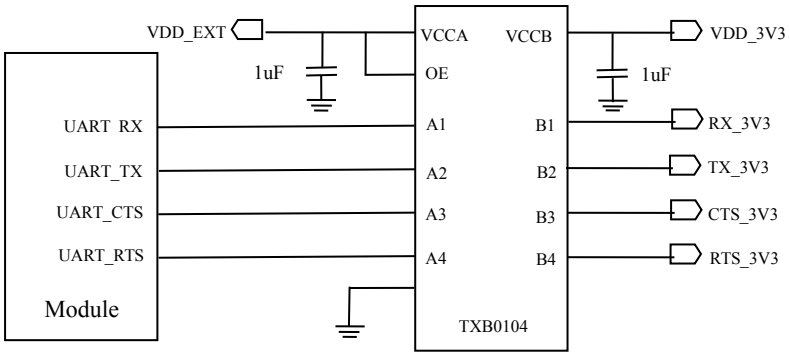

Figure 3- 13 Level conversion circuit

3.7 USIM interface

CLM920_TD5 Mini PCIE module provides a USIM card interface compatible with the ISO 7816-3 standard. The USIM card power provided by module's internal power manager and supports 1.8V/3.0V USIM card.

Table 3- 9 USIM Pin definitions

Pin	Signal name	I/O	High value	Description
6	UIM_DET	DI	1.8V	SIM hot-plug detection
8	UIM_PWR	PO	1.8V/2.85V	SIM card power supply
10	UIM_DATA	IO	1.8V/2.85V	SIM data signal
12	UIM_CLK	DO	1.8V/2.85V	SIM clock signal
14	UIM_RESET	DO	1.8V/2.85V	SIM reset signal

3.7.1 USIM card reference circuit

CLM920_TD5 Mini PCIE module without USIM card slot, users need to design a USIM card slot on your own interface card.
USIM card interface reference design diagram is as follow:

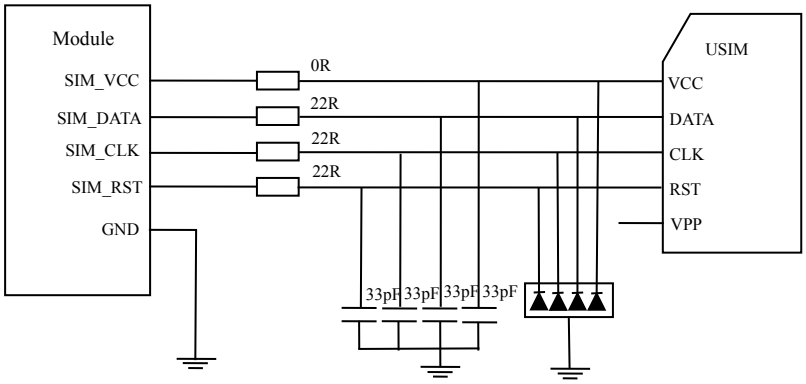

Figure 3- 14 USIM design circuit

NOTE

① Recommended ONSEMI company’s SMF15C for ESD protection on the interface line, peripheral circuit devices should be placed near the card slot. Keep layout of USIM card as close to the module as possible.

② USIM card will lost or become unavailable when disturbed by RF, so the USIM card slot should be placed away from the radio frequency radiation of the antenna, power and high speed signal lines.

③ UIM_DATA has connect to the VDD_EXT by the 47K resistance from internal, needn’t pull from external.

④ UIM_DET is the pin that check the USIM card is inserted or not. It is high by default and can detect the status of the SIM card through this PIN when hot plugging.

⑤ The 22R resistors should be added in series between the module and USIM card to avoid overload on USIM interface.

⑥ The gound of USIM slot and module have to maintian good connectivity.

3.7.2 UIM_DET Hot-Plug Reference Design

CLM920_TD5 Mini PCIE module supports SIM hot-plugging.
UIM_DET pin as an input detective pin to determine whether the SIM card is inserted or not. UIM_DET pin is pulled high by default.

Table 3- 10 SIM Hot-plug detective pins definitions

NO	UIM_DET state	Function description
1	high	SIM card is inserted, UIM_DET is high
2	low	SIM card is pulled out, UIM_DET is low

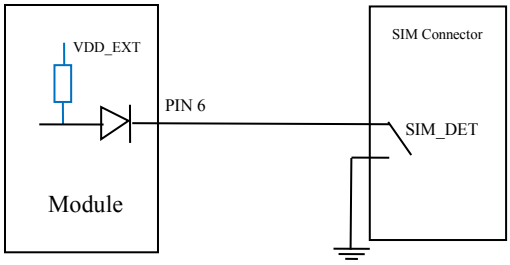

Figure 3- 15 Hot plugging of the USIM card

NOTE

① Recommended to add a diode protection next to the UIM _DET pin of the module.
② When using normally closed or normally open SIM card slot, the detection function can be set by AT command. If set AT + HOSCFG = 1,1 , the state is high when SIM card in place , set AT + HOSCFG = 1,0 , the state is low when SIM card in place and set AT+HOSCFG=0,0 to close the detective function.

3.8 General purpose GPIO interface

CLM920_TD5 Mini PCIE module includes three general control signal. The interfcae definitions as follows:

Table 3- 11 General GPIO Pin Definitions

Pin	Siganl name	I/O	High value	Description
19	WAKEUP_IN	DI	1.8V	Module sleep control
20	W_DISABLE#	DI	1.8V	Close RF
32	WAKEUP_OUT	DO		The module wakes up the host, open-drain

CLM920_TD5 Mini PCIE module supports sleep wake-up. WAKEUP_IN for the host control module sleep wake-up, WAKEUP_OUT for the module to wake up the host. (Use the command

AT^RPTFLAG=0 to enable the wake-up function when power on.)

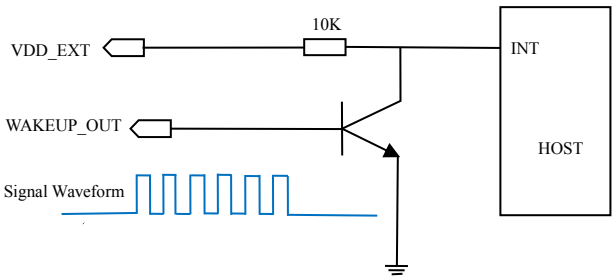

Figure 3- 16 WAKEUP_OUT signal wave

The host can awaken module when pull up CLM920_TD5 Mini PCIE module's WAKEUP_IN to 1.8V.

The module's RF will be colse when pull down the module's W_DISABLE# and the RF will be open when pull up the W_DISABLE#.

3.9 Network Indication Interface

CLM920_TD5 Mini PCIE module provides an open-drain GPIO signal to indicate RF communication status.

Table 3- 12 Network LED Pin Definition

Pin Name	Pin	I/O	Description
LED_WWAN#	42	PI	Network status indicator

Table 3- 13 Network indicator status

Status	LED display status
No service	Always bright
Modules are registered on non-4G networks	Flash slowly
Module registered on 4G network or module registered on non-4G network for voice SMS and other services	Flash fast

LED network indicator reference design is as follow:

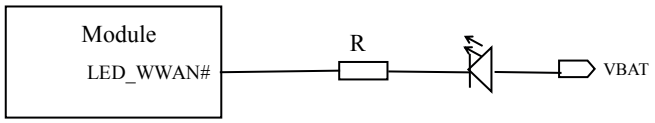

Figure 3- 17 network indicator circuit diagram

NOTE

LED light's brightness can be adjusted by limiting the value of resistance, the maximum current can be adjusted to 40mA .

3.10 Analog voice interface

CLM920_TD5 Mini PCIE module provides a set of analog voice interfaces, including one differential input signal (MIC + / MIC-) and one differential output signal (SPK + / SPK-).

3.10.1 Analog Voice Reference Design

Table 3- 14 Analog voice pin definitions

Pin	Signal Name	I/O	Description
1	MIC+	AI	Analog Audio input+
3	MIC-	AI	Analog Audio input-
5	SPK+/REC+	AO	Analog Audio output+
7	SPK-/REC-	AO	Analog Audio output-

3.10.2 Analog Voice Reference Design

CLM920_TD5 Mini PCIE module's analog voice reference design is as follow:

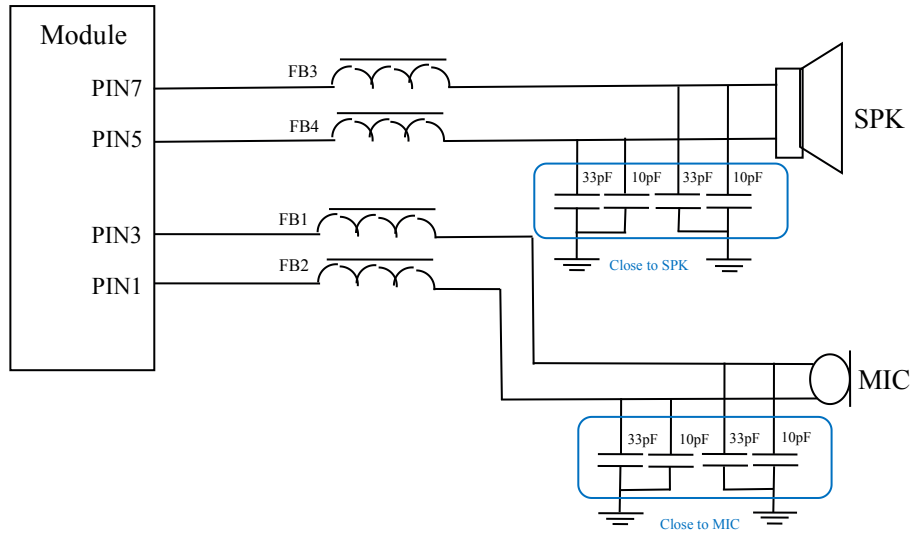

Figure 3- 18 Analog voice reference circuit

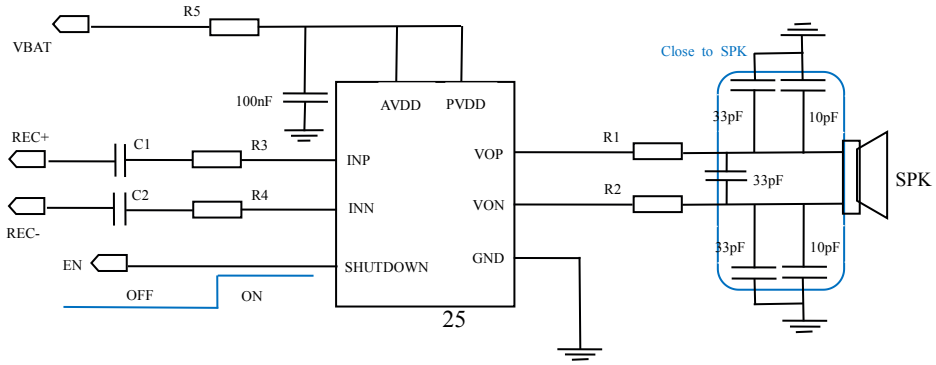

Figure 3- 19 External audio codec reference circuit

NOTE

① MIC + / MIC - channel used for the microphone differential input, module has provided microphone bias voltage for the operation from internal and external bias circuit is not needed. Mic usually use the electret microphone.

② SPK+/SPK- channel usually used for handset, headset or exteral power amplifier. When using exteral power amplifier, switch the module to headset output by AT+CSDVC=4, then connect the module to the external audio power amplifier signal.

③ The audio signal is a sensitive signal, the alignment should be careful to protect against interference, keep away from the RF interference area, connection lines as short as possible and protect sensitive signals when layout.

④ In order to prevent noise of TDD, design of audio circuit should reserved filter capacitance of 10 pF and 33 pF, which to remove radio frequency interference signal.

⑤ Users can set to handset output by AT+CSDVC=4, headset output by AT+CSDVC=2. Adjust the handset output volume gain by AT+COUTGAIN and set the Mic gain by AT+CMICGAIN. More details refer to the AT manual.

3.11 PCM audio interface

CLM920_TD5 Mini PCIE module provides one PCM audio interface, which supports 8-bit A-law and μ-law, 16-bit linear data formats, PCM_SYNC is 8kHZ, PCM_CLK is 2048kHZ。

Table 3- 15 PCM Pin Definition

Pin	Signal Name	I/O	Descripition
45	PCM_CLK	DO	PCM clock signal
47	PCM_DOUT	DO	PCM data output
49	PCM_DIN	DI	PCM data input
51	PCM_SYNC	DO	PCM frame sync

Table 3- 16 PCM Parameter

Feature	Descripition
Data Format	linear
Data bit	16bits
PCM role	Master/Slave
PCM Clock	2048kHz
PCM Frame Sync	short

Transfer	MSB

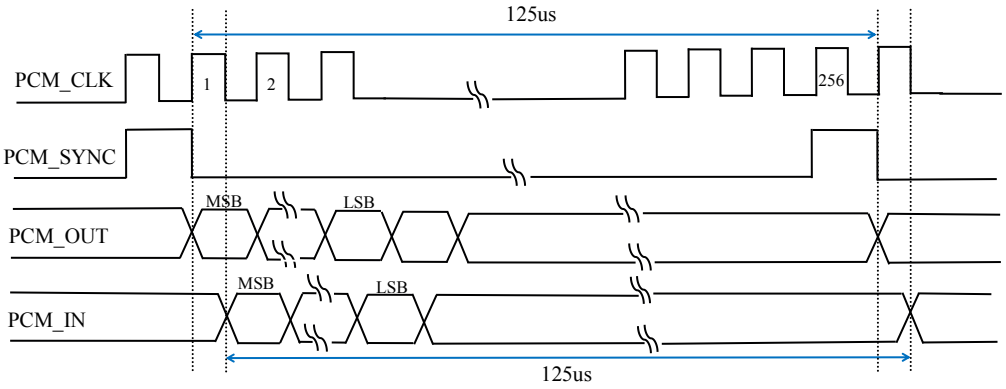

Figure 3- 20 PCM short mode sequence diagram

3.12 Antenna Interface

CLM920_TD5 Mini PCIE module has three antenna interfaces which include a main antenna interface, a Rx-diversity antenna interface and a GNSS antenna interface. Diversity antenna is recommended, which used to limit the signal drop by high speed moving or multipath fading.

3.12.1 RF Connector Location

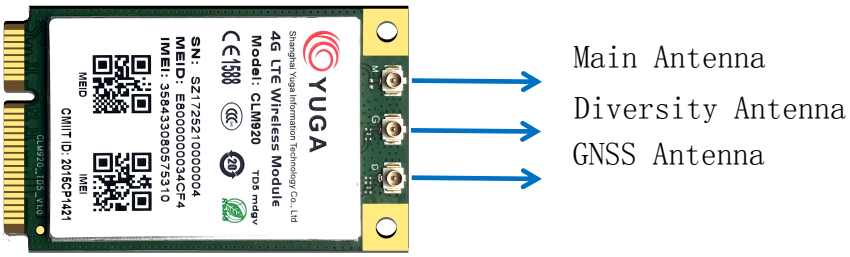

Figure 3- 21 RF connector location map

3.12.2 RF Connector

The connection mode of using RF Connector is recommended.

- ✧ The antenna connector must use a 50 Ω characteristic impedance coaxial connector and choose the RF cables which insertion loss as low as possible.
- ✧ It is recommended to use Murata's MM9329-2700 connector.

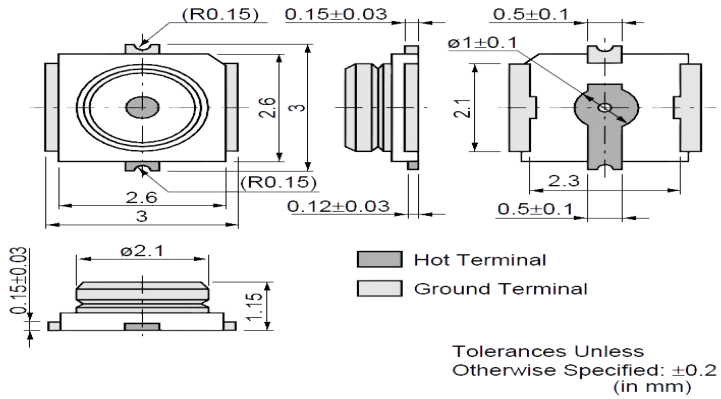

Figure 3- 22 RF connector dimensions

Table 3- 17 RF Connector Parameters

Rated condition		Environmental condition
Frequency Range	DC to 6GHZ	-40° C to +85° C
Characteristic impedance	50 Ω	-40° C to +85° C

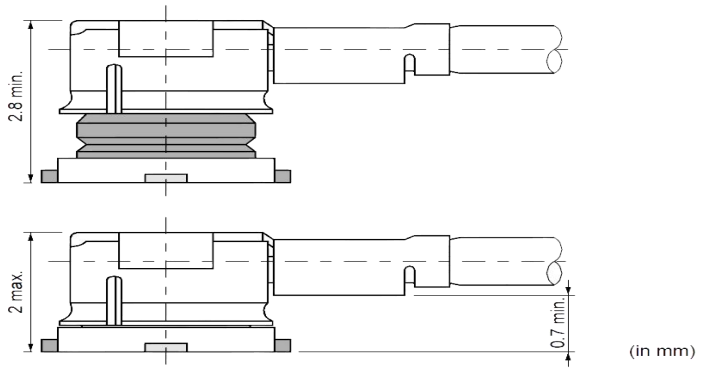

Figure 3- 23 Recommended Coaxial RF Cable Dimensions

NOTE

① CLM920_TD5 Mini PCIE module has three antenna interfaces which include a main antenna interface, a Rx-diversity antenna interface and a GNSS antenna interface(optional). The connection to the antenna must be a 50Ω characteristic impedance trace.

② The antenna matching circuit parameters can optimized by antenna factory based on the user's circuit board. Resistor R1/R2/R3/R4 is 0Ω by default and C1/C2/C3/C4 is empty by default.

③ To prevent electrostatic damage to the module's components, it is suggested that choosing a low capacitance ESD device PESD0542U015 to stick on the D1/D2 of the antenna connection.

Main Antenna

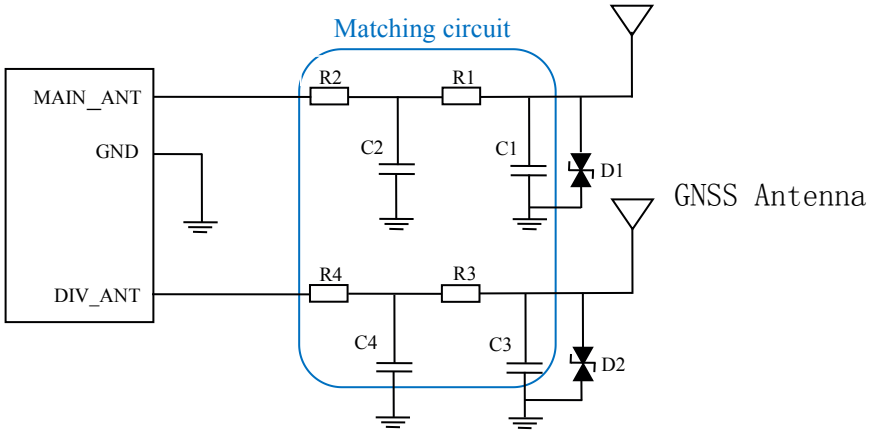

Figure 3- 24 Antenna matching circuit

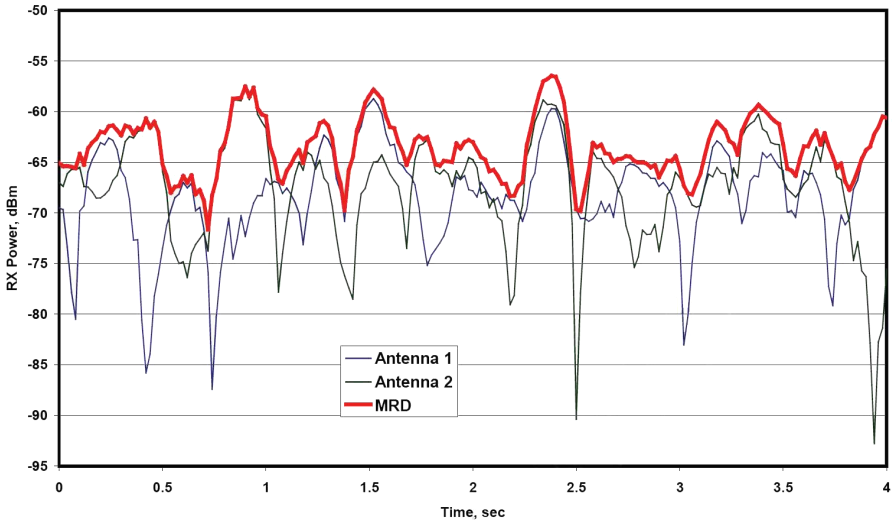

Figure 3- 25 Received signal strength with and without diversity antenna

4 Overall Technical Indicators

4.1 Overview of this chapter

CLM920_TD5 Mini PCIE module radio contains the following sections:

- ✧ Operating frequency ;
- ✧ Conducted RF measurements ;
- ✧ Conducted receiver sensitivity and transmit power;
- ✧ Operating current
- ✧ Antenna requirements

4.2 Operating frequency

Table 4- 1 RF Frequency Table

Frequency	Uplink frequency	Downlink frequency	Duplex mode

band			
LTE B1	1920MHz - 1980MHz	2110MHz - 2170MHz	FDD
LTE B2	1850MHz - 1910MHz	1930MHz - 1990MHz	FDD
LTE B3	1710MHz - 1785MHz	1805MHz - 1880MHz	FDD
LTE B4	1710MHz - 1755MHz	1950MHz - 2155MHz	FDD
LTE B5	824MHz - 849MHz	869MHz - 894MHz	FDD
LTE B7	2500MHz - 2570MHz	2620 MHz - 2690 MHz	FDD
LTE B8	880 MHz - 915 MHz	925 MHz - 960 MHz	FDD
LTE B17	704 MHz - 716 MHz	734 MHz - 746 MHz	FDD
LTE B20	832 MHz - 862 MHz	791 MHz - 821 MHz	FDD
LTE B28	703 MHz - 748 MHz	758 MHz - 803 MHz	FDD
LTE B38	2570MHz - 2620MHz	2570MHz - 2620MHz	TDD
LTE B39	1880MHz - 1920MHz	1880MHz - 1920MHz	TDD
LTE B40	2300MHz - 2400MHz	2300MHz - 2400MHz	TDD
LTE B41	2496MHz - 2690MHz	2496MHz - 2690MHz	TDD
GSM850	824MHz - 849MHz	869MHz - 894MHz	GSM
GSM900	880MHz - 915MHz	925MHz - 960MHz	GSM
DCS1800	1710MHz - 1785MHz	1805MHz - 1880MHz	GSM
PCS1900	1850MHz - 1910MHz	1930MHz - 1990MHz	GSM
UMTS B1	1920MHz - 1980MHz	2110MHz - 2170MHz	WCDMA
UMTS B2	1850MHz - 1910MHz	1930MHz - 1990MHz	WCDMA
UMTS B5	824MHz - 849MHz	869MHz - 894MHz	WCDMA
UMTS B8	880MHz - 915MHz	925MHz - 960MHz	WCDMA
BC0	824MHz - 849MHz	869MHz - 894MHz	CDMA
TDS B34	2010MHz - 2025MHz	2010MHz - 2025MHz	TD-SCDMA
TDS B39	1880MHz - 1920MHz	1880MHz - 1920MHz	TD-SCDMA

4.3 Conducted RF Measurements radio frequency

4.3.1 Test environment

Table 4- 2 Test Instruments

Test Instrument	power supply	Murata coaxial RF cable
R&S CMW500	Agilent 66319	MXHP32HP1000

4.3.2 Test standards

CLM920_TD5 Mini PCIE module passes the 3GPP TS 51.010-1, 3GPP TS 34.121-1, 3GPP

TS 36.521-1, 3GPP2 C.S0011 and 3GPP2 C.S0033 test standards. Each module pass the rigorous testing in the factory to ensure reliable quality.

4.4 Conducted receive sensitivity and transmit power

CLM920_TD5 Mini PCIE module’s 2G and 3G receiver sensitivity and transmit power test indicators are as follows:

Table 4- 3 2G 3G RF specifications

Mode	Up	Down	Power	Receiver sensitivity
GSM 850	824MHz - 849MHz	869MHz - 894MHz	33±2dBm	<-109dBm
GSM 900	880MHz - 915MHz	925MHz - 960MHz	33±2dBm	<-109dBm
DCS 1800	1710MHz-1785MHz	1805MHz - 1880MHz	30±2dBm	<-109dBm
PCS 1900	1850MHz-1910MHz	1930MHz - 1990MHz	30±2dBm	<-109dBm
WCDMA B1	1920MHz-1980MHz	2110MHz - 2170MHz	23+2/-2dBm	<-109dBm
WCDMA B2	1850MHz-1910MHz	1930MHz - 1990MHz	23+2/-2dBm	<-109dBm
WCDMA B5	824MHz - 849MHz	869MHz - 894MHz	23+2/-2dBm	<-109dBm
WCDMA B8	880MHz - 915MHz	925MHz - 960MHz	23+2/-2dBm	<-109dBm
TD-SCDMA B34	2010MHz-2025MHz	2010MHz - 2025MHz	24+1/-3dBm	<-109dBm
TD-SCDMA B39	1880MHz-1920MHz	1880MHz - 1920MHz	24+1/-3dBm	<-109dBm
EVDOrA	824MHz - 849MHz	869MHz - 894MHz	23+2/-2dBm	<-108dBm

CLM920_TD5 Mini PCIE Module’s 4G receiver sensitivity and transmit power test indicators are as follows:

Table 4- 4 4G RF sensitivity index

Directory (sensitivity)	3GPP protocol requirements	Min	Typical	Max
LTE B1 (FDD QPSK 通过) 95%)	< -96.3(10 MHz)		-99	-98
LTE B2 (FDD QPSK 通过) 95%)	< -94.3(10 MHz)		-97	-96
LTE B3 (FDD QPSK 通过) 95%)	< -93.3(10 MHz)		-96	-95
LTE B4 (FDD QPSK 通过) 95%)	< -96.3(10 MHz)		-98	-97
LTE B5 (FDD QPSK 通过) 95%)	< -94.3(10 MHz)		-97	-96
LTE B7 (TDD QPSK 通过) 95%)	< -94.3(10 MHz)		-97	-96
LTE B8 (TDD QPSK 通过) 95%)	< -93.3(10 MHz)		-97	-96
LTE B17 (TDD QPSK 通过) 95%)	< -93.3(10 MHz)		-96	-95

LTE B20（TDD QPSK 通过）95%）	＜ -93.3(10 MHz)	-96	-95
LTE B28（TDD QPSK 通过）95%）	＜ -94.8(10 MHz)	-97	-96
LTE B38（TDD QPSK 通过）95%）	＜ -96.3(10 MHz)	-98	-97
LTE B39（TDD QPSK 通过）95%）	＜ -96.3(10 MHz)	-99	-98
LTE B40（TDD QPSK 通过）95%）	＜ -96.3(10 MHz)	-99	-98
LTE B41（TDD QPSK 通过）95%）	＜ -96.3(10 MHz)	-98	-97

Table 4- 5 4G RF transmission power

Directory	3GPP protocol requirements (dBm)	Min	Typical	Max
LTE B1	21 to 25	22	23	24
LTE B2	21 to 25	22	23	24
LTE B3	21 to 25	22	23	24
LTE B4	21 to 25	22	23	24
LTE B5	21 to 25	22	23	24
LTE B7	21 to 25	22	23	24
LTE B8	21 to 25	22	23	24
LTE B17	21 to 25	22	23	24
LTE B20	21 to 25	22	23	24
LTE B28	21 to 25	22	23	24
LTE B38	21 to 25	22	23	24
LTE B39	21 to 25	22	23	24
LTE B40	21 to 25	22	23	24
LTE B41	21 to 25	22	23	24

4.5 Antenna requirements

CLM920_TD5 Mini PCIE Module’s antenna design requirements:

Table 4- 6 Main Antenna specifications

Frequency band	Standing wave ratio	Gain	Efficiency	TRP	TIS
GSM850	<2.5:1	〉-4dbi	〉40%	29	<-102
GSM900	<2.5:1	〉-4dbi	〉40%	29	<-102
DCS1800	<2.5:1	〉-4dbi	〉40%	26	<-102
PCS1900	<2.5:1	〉-4dbi	〉40%	26	<-102
B1 FDD	<2.5:1	〉-4dbi	〉40%	19	<-94
B2 FDD	<2.5:1	〉-4dbi	〉40%	19	<-94

B3 FDD	<2.5:1	〉-4dbi	〉40%	19	<-91
B4 FDD	<2.5:1	〉-4dbi	〉40%	19	<-92
B5 FDD	<2.5:1	〉-4dbi	〉40%	19	<-92
B7 FDD	<2.5:1	〉-4dbi	〉40%	19	<-92
B8 FDD	<2.5:1	〉-4dbi	〉40%	19	<-94
B17 FDD	<2.5:1	〉-4dbi	〉40%	19	<-94
B20 FDD	<2.5:1	〉-4dbi	〉40%	19	<-94
B28 FDD	<2.5:1	〉-4dbi	〉40%	19	<-94
B38 TDD	<2.5:1	〉-4dbi	〉40%	19	<-93
B39 TDD	<2.5:1	〉-4dbi	〉40%	19	<-93
B40 TDD	<2.5:1	〉-4dbi	〉40%	19	<-93
B41 TDD	<2.5:1	〉-4dbi	〉40%	19	<-93
WCDMA B1	<2.5:1	〉-4dbi	〉40%	19	<-106
WCDMA B2	<2.5:1	〉-4dbi	〉40%	19	<-106
WCDMA B5	<2.5:1	〉-4dbi	〉40%	19	<-106
WCDMA B8	<2.5:1	〉-4dbi	〉40%	19	<-106
EVDOrA	<2.5:1	〉-4dbi	〉40%	19	<-106
B34 TDS	<2.5:1	〉-4dbi	〉40%	19	<-106
B39 TDS	<2.5:1	〉-4dbi	〉40%	19	<-106

Table 4- 7 GNSS Antenna specifications

Frequency band	Standing wave ratio	Active noise factor	Active antenna gain	Active antenna embedded gain
GPS L1 1575.41+/1.023 MHZ	<2:1	<1.5DB	>-2DBi	20DB
GLONASS 1597.5-1605.8M HZ	<2:1	<1.5DB	>-2DBi	20DB
BeiDou 1559.05-1563.14MHZ	<2:1	<1.5DB	>-2DBi	20DB

4.6 Power consumption characteristics

Table 4- 8 GSM power consumption

Frequency band	Configuration	Power rating	Current consumption (mA)
GPRS850	1UP/1DL	5	310

GPRS900	1UP/1DL	5	315
GPRS1800	1UP/1DL	0	200
GPRS1900	1UP/1DL	0	192
EDGE850	1UP/1DL	8	220
EDGE900	1UP/1DL	8	225
EDGE1800	1UP/1DL	2	175
EDGE1900	1UP/1DL	2	170

Table 4- 9 WCDMA power consumption

Frequency band	Power(dbm)	Current consumption(mA)
WCDMA B1	23.2	556
WCDMA B1	1	165
WCDMA B2	23.7	556
WCDMA B2	1.2	165
WCDMA B5	22.6	590
WCDMA B5	1	152
WCDMA B8	22.4	532
WCDMA B8	1	144

Table 4- 10 LTE power consumption

Frequency band	Power(dbm)	Current consumption(mA)
B1	21.5	562
B2	23.6	608
B3	21.8	590
B4	23.3	618
B5	22.5	575
B7	22.1	597
B8	23.2	562
B17	23	550
B20	23.5	571
B28	22.8	567
B38	22.5	465
B39	21.9	375
B40	22.1	362
B41	22.8	482

Table 4- 11 TDS-CDMA power consumption

Frequency band	Power(dbm)	Current consumption(mA)
TDS B34	22.8	173
TDS B39	23.1	180

Table 4- 12 CDMA power consumption

Frequency band	Power(dbm)	Current consumption(mA)
BC0	24	621

5 Interface electrical characteristics

5.1 Operating Storage Temperature

Table 5- 1 4G module operation and storage temperature

Parameter	Min	Max
Normal working temperature	-35° C	75° C
Limit working temperature	-40° C	85° C
Storage temperature	-45° C	90° C

5.2 Module IO electrical characteristics

CLM920_TD5 Mini PCIE module's IO level is as follows:
The UIM_PWR is 1.8V for a 1.8V USIM application and 2.85V for a 3V USIM application.
The other digital IO levels are unified to 1.8V.

Table 5- 2 CLM920_TD5 Mini PCIE Module IO Electrical Characteristics

Parameter	Parameter Description	Min	Max
VIH	High level input voltage	0.65* VDD_EXT	VDD_EXT+0.3V
VIL	Low level input voltage	-	0.35*VDD_EXT
VOH	High level output voltage	VDD_EXT-0.45V	VDD_EXT
VOL	Low level output voltage	0	0.45V

5.3 Power supply characteristics

CLM920_TD5 Mini PCIE module's input power supply requirements are as follows:

Table 5- 3 CLM920_TD5 Mini PCIE module operating characteristics

Parameter	Min	Typical	Max
VBAT	3.3V	3.7V	4.2V
UIM_PWR	1.7V/2.75V	1.8V/2.85V	1.9V/2.95V

NOTE

The power-on time of any interface of the module must not be earlier than the power-on time of the module. Otherwise, the module may be abnormal or damaged.

5.4 Electrostatic characteristics

CLM920_TD5 Mini PCIE module requires ESD protection to ensure product quality in using.

Table 5- 4 CLM920_TD5 ESD Characteristics

Test port	Contact discharge	Air discharge	Unit
USB interface	±4	±8	KV
USIM interface	±4	±8	KV
Analog voice interface	±4	±8	KV
VBAT Power supply	±4	±8	KV

6 Structural and mechanical properties

6.1 Appearance

CLM920_TD5 Mini PCIE module is a double-sided PCBA . The appearance of the module is as below :

Figure 6- 1 CLM920_TD5 appearance

6.2 Mini PCI Express connector

CLM920_TD5 Mini PCIE module interface meets the PCI Express Mini Card 1.2 interface standard, PCI Express Mini Card connectors conforming to this standard can be used, such as Molex 679100002.

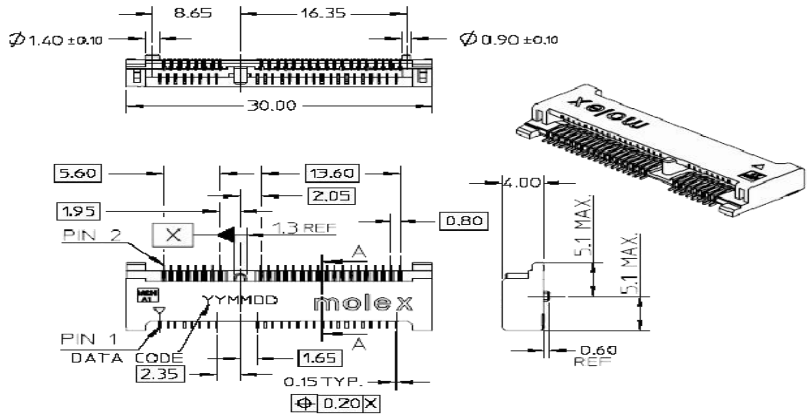

Figure 6- 2 Connector dimensions

6.3 Module fixing method

CLM920_TD5 Mini PCIE module is fixed with two grounding screw holes.