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CLM920 TD3 LTE Module Hardware Usage Guide

V1.0

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Chapter 1 Introduction

This document is a hardware solution manual for the wireless solution product CLM920 TD3 module. It is intended to describe the hardware components and functional characteristics of the module solution, application interface definition and usage instructions, electrical performance and mechanical characteristics. Combined with this and other application documents, users can quickly use this module to design wireless products.

Chapter 2 Module review

2.1 Module introduction

The CLM920 TD3 module is an LCC package module. It is a wireless terminal product that integrates various network standards and GPS positioning services such as FDD-LTD/ TDD-LTE/WCDMA/EDGE/GSM. The module is based on Qualcomm MDM9X07 chip development, supports Cat4, uplink and downlink speeds up to 50Mbps/150Mbps, and fully supports VOLTE and SRLTE, and supports embedded operating systems such as Windows7/Windows8/Windows10/Android/Linux.

The CLM920 TD3 module can be used in the following applications:

- ✧ Car Equipment
- ✧ Wireless POS machine
- ✧ Wireless advertising, multimedia
- ✧ Remote monitoring
- ✧ Smart meter reading
- ✧ Mobile broadband
- ✧ automated industry
- ✧ Other wireless terminals, etc.

2.2 Module characteristics

Table 2-1 List of module bands

Network Type	Frequency band	Module series	
		CLM920 TD3_na American version	CLM920 TD3_au Australian version
GSM	GSM850	●	●
	GSM900	●	●
	GSM1800	●	●
	GSM1900	●	●
LTE(FDD)	LTE FDD B1		●
	LTE FDD B2	●	●
	LTE FDD B3	●	●
	LTE FDD B4	●	
	LTE FDD B5	●	●

	LTE FDD B7	●	●
	LTE FDD B8	●	●
	LTE FDD B12	●	
	LTE FDD B13	●	
	LTE FDD B17	●	
	LTE FDD B25	●	
	LTE FDD B26	●	
	LTE FDD B28		●
	LTE FDD B66	●	
LTE(TDD)	LTE TDD B40		●
	LTETDDB41 (Narrow Band)	●	
WCDMA	BAND 1		●
	BAND 2	●	●
	BAND 4	●	
	BAND 5	●	●
	BAND 8	●	●
GNSS	GLONASS	●	●
	GPS	●	●
	BeiDou/Compass	●	●

NOTE

- ✧ The module does not support diversity, GPS, and voice functions by default.
- ✧ The GNSS function is optional.
- ✧ The diversity function is optional.
- ✧ Voice function (digital voice).
- ✧ The CLM920 TD3 supports CAT1 standard modules for customer-specific applications. The CAT1 system has an uplink of 5 Mbps and a downlink of 10 Mbps.
- ✧ The module supports Category4 by default. When the Category1 module needs to be supported, the CLM920 TB3 cat1 is printed on the module label.
- ✧ CAT1 does not support diversity.

Table 2-2 Key Features

Characteristic		Description
Physical characteristics		32mm x 29mm x 2.4mm
Fixed way		LCC package, patch mount
Operating Voltage		3.3V - 4.2V Typical Voltage 3.7V
Energy saving current		Standby current < 5mA
Application interface	Standard SIM interface	Support 3.0V/1.8V, support hot swap function
	USB2.0	USB2.0 (High-Speed) (only supports slave mode), data transfer rate up to 480Mbps For AT commands, data transfer, GNSS NMEA output, software debugging and software upgrades USB driver: Support Windows XP, Windows Vista, Windows 7, Windows 10, Windows CE 5.0/6.0/7.0 Linux 2.6 or higher Android 2.3/4.0/4.2/4.4/5.0/6.0/7.1, etc.
	Hardware reset interface	Used to reset the module, low effective
	UART serial interface	Main serial port (8 lines): For AT commands and data transfer The baud rate is up to 921600bps and the default is 115200bps. Support RTS and CTS hardware flow control Debug serial port (2 lines): Used to print module logs
	PCM interface	For audio, requires an external codec chip Supports 8-bit A-law, U-law and 16-bit linear encoding formats Support short frame mode Support main mode
	SPI interface	Maximum clock rate up to 26MHz SPI can only be used as the master, the interface voltage domain is 1.8V Reusable I2S interface for external CODEC
	SD card interface	4-bit SD/MMC interface Clock frequency up to 50MHz

		Maximum capacity supports 32GB Interface voltage domain is 1.8/2.95V, two voltages are adjustable
	Power interface	Support 3.3V-4.2V DC power supply
	Network status indication	Used to indicate the status of the module, the speed of the light is on to indicate different module status
	General purpose GPIO interface	WAKEUP_IN sleep mode control, low level wake-up module AP_READY sleep state detection W_DISABLE# flight mode control
Transmit power		LTE: Class 3(23dBm±2dB) UMTS: Class 3(24dBm+1/-3dB) GSM/GPRS: Class 4(33dBm±2dB) GSM850/GSM900 Class 1(30dBm±2dB) DCS1800/PCS1900
Data service		GSM/EDGE: GPRS: DL 85.6kbps/UL 85.6kbps EDGE: DL 236.8kbps/UL 236.8kbps WCDMA: UMTS R99: DL 384kbps/UL 384kbps DC-HSPA+: DL 42Mbps/UL 5.76Mbps LTE: LTE FDD:DL 150Mbps/UL 50Mbps@20M BW cat4 LTE TDD:DL 130Mbps/UL 35Mbps@20M BW cat4 LTE FDD:DL 10Mbps/UL 5Mbps@20M BW cat1 LTE TDD:DL 10Mbps/UL 5Mbps@20M BW cat1
Satellite positioning		GPS/BEIDOU/GLONASS Protocol:NMEA
Diversity antenna		Support LTE diversity antenna
AT command		Support for standard AT instruction sets (Hayes 3GPP TS 27.007 and 27.005) Specific AT query CLM920 TD3 AT instruction set

SMS business	Support Text and PDU mode Support point-to-point MO and MT SMS storage: USIM card / ME (default)
Virtual network card	Support USB virtual network card
Temperature range	Normal operating temperature -30 ° C to +75 ° C Extreme operating temperature -40° C to +85° C
Storage temperature	-40° C to +85° C
Humidity	RH5%～RH95%
Module function distinction	On the label paper, M stands for the main set, D takes the table diversity, and G stands for GPS.

NOTE

When the temperature is in the range of －40° C to －30° C or +75° C to +85° C, some RF indicators of the CLM920 TD3 module may not meet the 3GPP standards.

2.3 Module function

The CLM920 TD3 LCC module mainly contains the following circuit units:

- ✧ Baseband processing unit
- ✧ Power management unit
- ✧ Memory unit
- ✧ RF transceiver unit
- ✧ RF front end unit
- ✧ GPS RF receiving unit

The functional block diagram of the CLM920 TD3 LCC module is shown below：

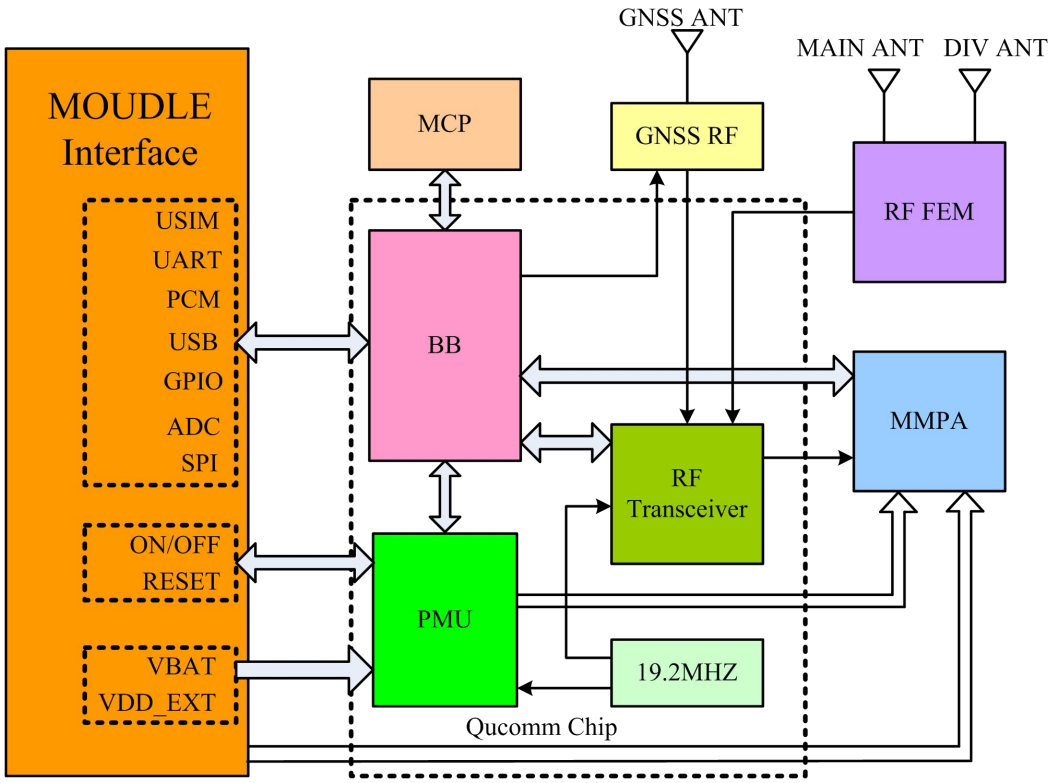


Figure 2-1 Functional block diagram of the CLM920 TD3 LCC module

Chapter 3 Interface application description

3.1 Chapter overview

This chapter mainly describes the interface definition and application of this module. Contains the following sections:

- 144 pin pin definition map
- Interface definition
- Power interface
- USB interface
- USIM interface
- UART interface
- Control interface
- PCM/I2S voice interface
- RF antenna interface
- GPIO interface
- WLAN interface
- SGMII interface
- Reserved
- NC interface
- SPI interface
- SDIO interface

3.2 Module interface

3.2.1 144-pin LCC interface

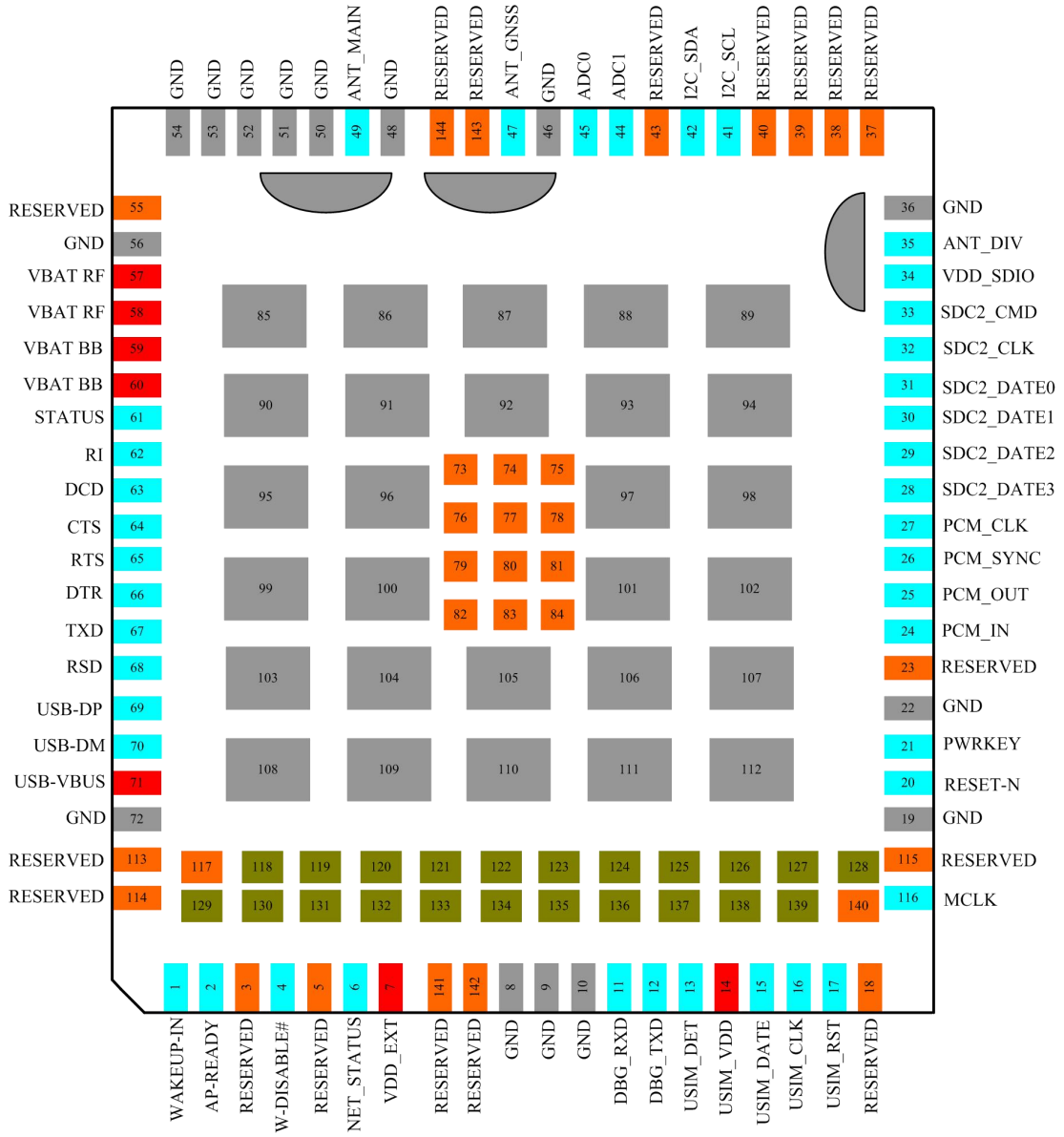


Figure 3-1 LCC module interface definition

3.2.2 Interface definition

The CLM920_TD3 module interface is an LCC interface module. The module interface is defined as shown in the following table.:

Table 3-1 Pin definitions

Pin	Pin name	Pin	Pin name
1	WAKEUP_IN	2	AP_READY
3	GPIO_1	4	W_DISABLE#

5	GPIO_2	6	NET_STATUS
7	VDD_EXT	8	GND
9	GND	10	GND
11	DBG_RXD	12	DBG_TXD
13	USIM_DET	14	USIM_VDD
15	USIM_DATA	16	USIM_CLK
17	USIM_RST	18	RESERVED
19	GND	20	RESET_N
21	PWRKEY	22	GND
23	RESERVED	24	PCM_IN
25	PCM_OUT	26	PCM_SYNC
27	PCM_CLK	28	SDC2_DATA3
29	SDC2_DATA2	30	SDC2_DATA1
31	SDC2_DATA0	32	SDC2_CLK
33	SDC2_CMD	34	VDD_SDIO
35	ANT_DIV	36	GND
37	SPI_CS_N(I2S_D1)	38	SPI_MOSI(I2S_WS)
39	SPI_MISO(I2S_D0)	40	SPI_CLK(I2S_SCLK)
41	I2C_SCL	42	I2C_SDA
43	RESERVED	44	ADC1
45	ADC0	46	GND
47	ANT_GNSS	48	GND
49	ANT_MAIN	50	GND
51	GND	52	GND
53	GND	54	GND
55	RESERVED	56	GND
57	VBAT	58	VBAT
59	VBAT	60	VBAT
61	STATUS	62	RI
63	DCD	64	CTS
65	RTS	66	DTR
67	TXD	68	RXD

69	USB_DP	70	USB_DM
71	USB_VBUS	72	GND
73	RESERVED	74	RESERVED
75	RESERVED	76	RESERVED
77	RESERVED	78	RESERVED
79	RESERVED	80	RESERVED
81	RESERVED	82	RESERVED
83	RESERVED	84	RESERVED
85	GND	86	GND
87	GND	88	GND
89	GND	90	GND
91	GND	92	GND
93	GND	94	GND
95	GND	96	GND
97	GND	98	GND
99	GND	100	GND
101	GND	102	GND
103	GND	104	GND
105	GND	106	GND
107	GND	108	GND
109	GND	110	GND
111	GND	112	GND
113	RESERVED	114	RESERVED
115	RESERVED	116	MCLK
117	RESERVED	118	WLAN_SLP_CLK
119	EPHY_RST_N	120	EPH_INT_N
121	SGMII_MDATA	122	SGMII_MCLK
123	SGMII_TX_M	124	SGMII_TX_P
125	SGMII_RX_P	126	SGMII_RX_M
127	WLAN_3.3V_EN	128	USIM2_VDD
129	SDC1_DATA3	130	SDC1_DATA2
131	SDC1_DATA1	132	SDC1_DATA0

133	SDC1_CLK	134	SDC1_CMD
135	WAKE_WLAN	136	SDC1_EN
137	COEX_UART_RXD	138	COEX_UART_TXD
139	RESERVED	140	RESERVED
141	RESERVED	142	RESERVED
143	RESERVED	144	RESERVED

Table 3-2 IO parameter definition

Symbol sign	Description
IO	Two-way input and output
PI	power input
PO	Power Output
AI	Analog input
AO	Analog output
DI	Digital input
DO	Digital output
OD	Leaky open circuit

Table 3-3 Pin description

Power supply				
Pin	Pin definition	IO	Functional description	Remarks
57	VBAT	PI	Module power input	Power supply needs to guarantee 2A current
58	VBAT	PI	Module power input	
59	VBAT	PI	Module power input	
60	VBAT	PI	Module power input	
7	VDD_EXT	PO	1.8V output	Can provide pull-up (maximum 50MA) for external GPIO. Please keep it floating when not in use.

8,9,10,19,22,36,46,48, 50,51,52,53,54,56,72	GND		Ground	
85~112	GND		Heat sink pad	

Module switch machine and reset				
Pin	Pin definition	IO	Functional description	Remarks
21	PWRKEY	DI	Switching module pin	Active low
20	RESET	DI	Module reset pin	Low level reset module

USB interface				
Pin	Pin definition	IO	Functional description	Remarks
71	USB_VBUS	PI	USB detection	
69	USB_D+	IO	USB bus differential positive signal	90Ω differential impedance
70	USB_D-	IO	USB bus differential negative signal	90Ω differential impedance

UART interface (main serial port)				
Pin	Pin definition	IO	Functional description	Remarks
62	RI	DO	Ringing prompt	Wake up the host, please keep it floating when not in use
63	DCD	DO	Carrier detection	please keep it floating when not in use
64	CTS	DO	Clear send	please keep it floating when not in use
65	RTS	DI	Request to send	please keep it floating when not in use
66	DTR	DI	Module sleep mode control	please keep it floating when not in use
67	TXD	DO	Serial data transmission	please keep it floating when not in use
68	RXD	DI	Serial data reception	please keep it floating

				when not in use
Debug serial port				
11	DBG_RXD	DI	Serial data reception	please keep it floating when not in use
12	DBG_TXD	DO	Serial data transmission	please keep it floating when not in use

USIM interface				
Pin	Pin definition	IO	Functional description	Remarks
13	USIM_DET	DI	USIM card detection	please keep it floating when not in use
14	USIM_VDD	PO	USIM card power supply	Module automatically recognizes 1.8V or 3V USIM card
15	USIM_DATA	IO	USIM card data	
16	USIM_CLK	DO	USIM card clock	
17	USIM_RST	DO	USIM card reset	

GPIO pin				
Pin	Pin definition	IO	Functional description	Remarks
1	WAKEUP_IN	DI	Sleep mode control	
2	AP_READY	DI	Sleep state detection	During development (keep empty when not in use)
3	GPIO_1	IO	This pin function has not been defined	RESERVE, please keep it floating
4	W_DISABLE#	DI	Flight mode control	During development (keep empty when not in use)
5	GPIO_2	PI	This pin function has not been defined	RESERVE, please keep it floating

Module status indication interface				
Pin	Pin definition	IO	Functional description	Remarks
6	NET_STATUS	OD	Module work network status	please keep it floating

			light indication	when not in use
61	STATUS	DO	Module running status indication	please keep it floating when not in use

PCM interface				
Pin	Pin definition	IO	Functional description	Remarks
24	PCM_IN	DI	PCM receiving data	please keep it floating when not in use
25	PCM_OUT	DO	PCM interface	please keep it floating when not in use
26	PCM_SYNC	IO	PCM frame sync signal	please keep it floating when not in use
27	PCM_CLK	IO	PCM clock pulse	please keep it floating when not in use

SPI interface				
Pin	Pin definition	IO	Functional description	Remarks
37	SPI_CS_N	DO	SPI chip selection	Reuse I2S_D1 (please keep it floating when not in use)
38	SPI_MOSI	DO	SPI data output	Reuse I2S_WS (please keep it floating when not in use)
39	SPI_MISO	DI	SPI data input	Reuse I2S_D0 (please keep it floating when not in use)
40	SPI_CLK	DO	SPI clock	Reuse I2S_SCLK (please keep it floating when not in use)

MCLK				
Pin	Pin definition	IO	Functional description	Remarks
116	MCLK	DO	12.288M clock output	please keep it floating when not in use

ADC interface

Pin	Pin definition	IO	Functional description	Remarks
44	ADC1	AI	General analog to digital conversion	please keep it floating when not in use
45	ADC0	AI	General analog to digital conversion	please keep it floating when not in use

RF interface				
Pin	Pin definition	IO	Functional description	Remarks
35	ANT_DIV	AI	Diversity antenna	50Ω characteristic impedance(please keep it floating when not in use)
47	ANT_GNSS	AI	GNSS antenna	50Ω characteristic impedance(please keep it floating when not in use)
49	ANT_MAIN	IO	Main antenna	50Ω characteristic impedance

WLAN interface				
Pin	Pin definition	IO	Functional description	Remarks
127	PM_ENABLE	DO	Power enable	please keep it floating when not in use
129	SDC1_DATA3	IO	Data bus DATA3	please keep it floating when not in use
130	SDC1_DATA2	IO	Data bus DATA2	please keep it floating when not in use
131	SDC1_DATA1	IO	Data bus DATA1	please keep it floating when not in use
132	SDC1_DATA0	IO	Data bus DATA0	please keep it floating when not in use
133	SDC1_CLK	DO	WLAN clock	please keep it floating when not in use
134	SDC1_CMD	IO	WLAN command	please keep it floating when not in use
136	WLAN_EN	DO	WLAN enable	please keep it floating

				when not in use
118	WLAN_SLP_CLK	DO	WLAN sleep clock	please keep it floating when not in use
135	WAKE_WLAN	DI	WLAN wake-up module	please keep it floating when not in use
137	COEX_UART_RXD	DI	WLAN coexistence reception	please keep it floating when not in use
138	COEX_UART_TXD	DO	WLAN coexistence transmission	please keep it floating when not in use

SGMII interface				
Pin	Pin definition	IO	Functional description	Remarks
119	EPHY_RST_N	DO	Ethernet PHY reset	1.8V/2.85 voltage domain
120	EPH_INT_N	DI	Ethernet PHY interrupt	1.8 voltage domain
121	SGMII_MDATA	IO	SGMII MDIO data	1.8V/2.85 voltage domain
122	SGMII_MCLK	DO	SGMII MDIO clock	1.8V/2.85 voltage domain
128	USIM2_VDD	PO	SGMII_MDATA pull-up power supply	1.8V/2.85 voltage domain
123	SGMII_TX_M	AO	SGMII differential data transmission negative signal	Connect 0.1uF capacitors close to the chip end
124	SGMII_TX_P	AO	SGMII differential data transmission positive signal	Connect 0.1uF capacitors close to the chip end
125	SGMII_RX_P	AI	SGMII differential data receiving positive signal	Connect 0.1uF capacitors close to the module end
126	SGMII_RX_M	AI	SGMII differential data receiving negative signal	Connect 0.1uF capacitors close to the module end

RESERVE pin			
Pin number	Pin definition	Description	Remarks
18，23，28，29，30，31，32，33，34，37，38，39，40，43，55，73，74，75，76，77，78，79，80，81，	RESERVED	Reserve pins, please keep open	Please keep it floating

82，83，84 , 113, 114,117,139-144			

NOTE

- ✧ The module typically has an IO port level of 1.8V (in addition to the SIM, the SIM card port level supports 1.8V and 3.0V).
- ✧ This module defines the RESERVED and NC pins to be left floating and must not be used.

Functional multiplexing						
Pin	Pin name	Mode 1 (default)	Mode 2 (GPIO)	Mode 3	Functional description	Whether openLinux can be opened
1	WAKEUP_IN	WAKEUP_IN	GPIO_25			NO
2	AP_READY	AP_READY	GPIO_10			NO
3	GPIO_1	GPIO_1	GPIO_42			NO
4	W_DISABLE	W_DISABLE	GPIO_11			YES
5	GPIO_2	GPIO_24				NO
6	NET_STATUS	NET_STATUS	GPIO_19			NO
7	VDD_EXT	VDD_EXT				
11	DBG_RXD	DBG_RXD	GPIO_09			NO
12	DBG_TXD	DBG_TXD	GPIO_08			NO
13	USIM_DET	USIM_DET			SIM	
14	USIM_VDD	USIM_VDD				
15	USIM_DATA	USIM_DATA				
16	USIM_CLK	USIM_CLK				
17	USIM_RST	USIM_RST				
116	MCLK	MCLK				
115	FORCE_USB_BOOT	FORCE_USB_BOOT				
20	RESET_N	RESET_N				
21	PWRKEY	PWRKEY				
24	PCM_IN	PCM_IN	GPIO_76			NO

25	PCM_OUT	PCM_OUT	GPIO_77		PCM	NO
26	PCM_SYNC	PCM_SYNC	GPIO_79			NO
27	PCM_CLK	PCM_CLK	GPIO_78			NO
28	SDC2_DATA3	SDC2_DATA3				
29	SDC2_DATA2	SDC2_DATA2				
30	SDC2_DATA1	SDC2_DATA1			SD	
31	SDC2_DATA0	SDC2_DATA0				
32	SDC2_CLK	SDC2_CLK				
33	SDC2_CMD	SDC2_CMD				
34	VDD_SDIO	VDD_SDIO				
37	SPI_CS_N	SPI_CS_N	GPIO_22		SPI	NO
38	SPI_MOSI	SPI_MOSI	GPIO_20			NO
39	SPI_MISO	SPI_MISO	GPIO_21			NO
40	SPI_CLK	SPI_CLK	GPIO_23			NO
41	I2C_SCL	I2C_SCL	GPIO_07		I2C	YES
42	I2C_SDA	I2C_SDA	GPIO_06			YES
44	ADC1	ADC1	MPP_06			
45	ADC0	ADC0	PA_THERM2			
61	STATUS	STATUS	MPP_GPIO_04			
62	RI	RI	GPIO_75		UART	NO
63	DCD	DCD	GPIO_04			YES
64	CTS	CTS	GPIO_02			NO
65	RTS	RTS	GPIO_03			YES
66	DTR	DTR	GPIO_05			YES
67	TXD	TXD	GPIO_00			YES
68	RXD	RXD	GPIO_01			YES

69	USB_DP	USB_DP			USB	
70	USB_DM	USB_DM				

3.3 Power interface

- ✧ The CLM920 TD3 module power interface consists of three parts:
- ✧ VBAT is the module working power supply
- ✧ UIM_PWR is the working power supply for SIM card
- ✧ VDD_EXT is 1.8V output power (50mA)
- ✧ VDD_SDIO is the SD card pull-up power supply (50mA)

3.3.1 Power supply design

CLM920 TD3 module power interface is as follows：

Table 3-4 Power pin definitions

Pin	Name	I/O	Description	Min	Typical	Max
57,58,59,60	VBAT	PI	Module power supply	3.3V	3.7V	4.2V
14	UIM_PWR	PO	SIM power supply	0	1.8V/2.85V	1.98/3.3V
7	VDD_EXT	PO	Output power		1.8V	
34	VDD_SDIO	PO	Output power		1.8V/2.85V	
8,9,10,19,22,36,46,48,50,51,52,53,54,56,72,85~112	GND		Ground	-	0	-

The CLM920 TD3 module is powered by a single power supply and the module provides four power supply pins. The VBAT power supply range is 3.3-4.2V, and it is recommended to use 3.7V/2A power supply. When transmitting data or talking under HSPA/UTMS/GSM network, the instantaneous high-power transmission will produce a peak current of more than 2A peak, which will cause a large ripple on the power supply. If the instantaneous voltage drop causes the VBAT supply voltage to be too low. Or the supply current is insufficient and the module may shut down or restart. In order to ensure the normal operation of the module,

all power pins and ground pins must be connected and provide sufficient power supply capability.

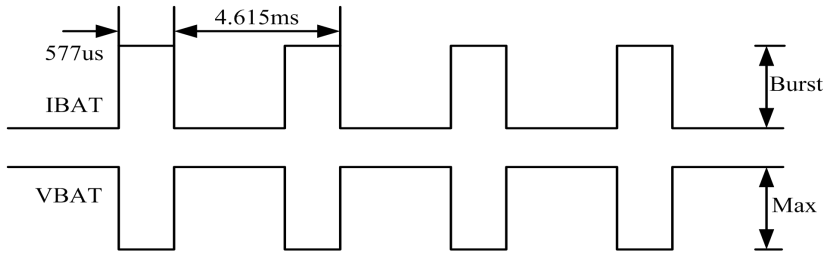


Figure 3-2 GSM TDMA network burst current supply voltage drop

Under the premise of ensuring that the VBAT power supply is sufficient, two 470uF/6.3V tantalum capacitors can be connected in parallel with the power input, and then 10pF, 33pF, 0.1uF, 1uF ceramic capacitors can be connected.

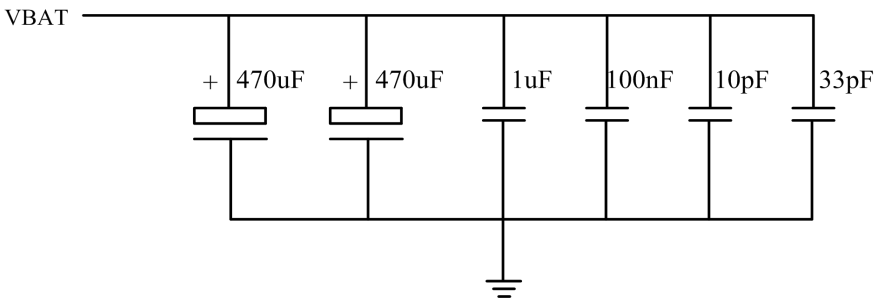


Figure 3-3 VBAT power supply

3.3.2 Power reference circuit

The actual design of the power circuit can use a switching DC power supply or a linear LDO power supply to design the VBAT power supply. Both design circuits need to supply enough current. Specific reference to the following circuit design：

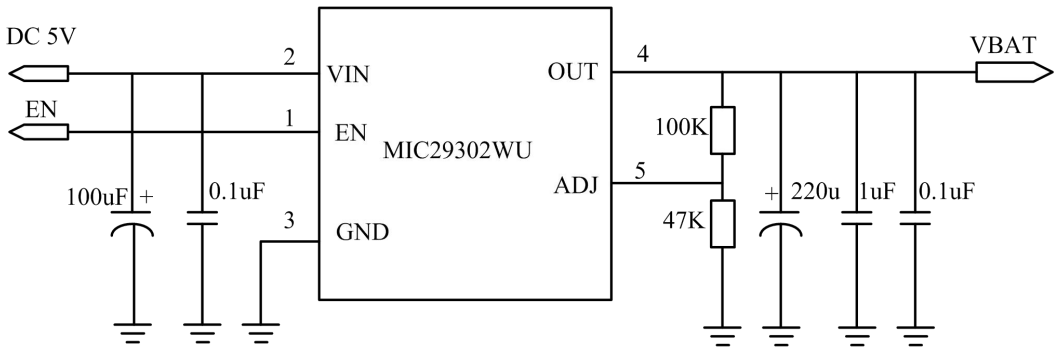


Figure 3-4 LDO linear power supply reference circuit

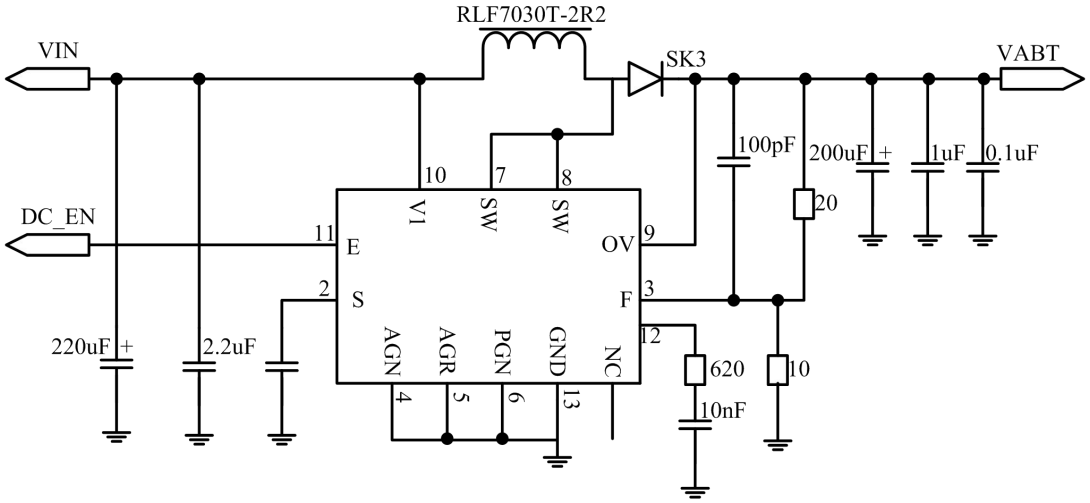


Figure 3-5 DC switching power supply reference circuit

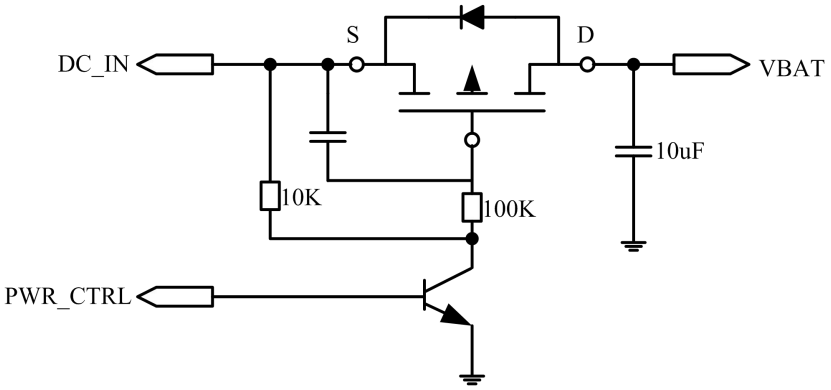


Figure 3-6 PMOS tube control power switch reference circuit

NOTE

- ✧ To prevent damage to the module from surges and overvoltages, it is recommended to connect a 5.1V/500mW Zener diode to the VBAT pin of the module.
- ✧ It is recommended to add 3 ceramic capacitors (33pF, 10pF, 100nF) to the VBAT pin and place them near the VBAT pin.
- ✧ The minimum operating voltage of the module is 3.3V. Since the transmission data or GSM call will generate more than 2A current, the ripple voltage drop will occur on the power supply voltage, so the actual supply voltage must not be lower than 3.3V.

3.3.3 VDD_SDIO 1.8V/2.85V Voltage output

Module output VDD_SDIO voltage is 2.85V/1.8V configurable, default is 2.85V, maximum output current is 50mA, can only be used for SDIO bus pull-up, SD card power supply needs to be provided from outside the module.

3.3.4 VDD_EXT 1V8 Voltage output

After the CLM920 TD3 module is powered on normally, the 17th pin will output 1.8V and the current load will be 50mA. The external master can read the voltage of VDD_EXT to judge whether the module is powered on. VDD_EXT can also be used as an external power supply, such as a level shifting chip.

3.4 Switching machine reset mode

3.4.1 Boot

The 21 pin of the CLM920 TD3 module is the boot pin. The module is powered on at low level. The PWRKEY is pulled low for at least 500ms. When the module is powered on, the user can check whether the module is powered on by querying the high and low levels of the VDD_EXT pin.

When the CLM920 TD3 module is powered on, pull the PWRKEY pin low for at least 1S and release it. The module will perform shutdown process shutdown (this function is under development).

Table 3-5 Switching machine pin definition

Pin	Signal name	I/O	High value	Description
21	PWRKEY	PI	VBAT-0.3V	Low level boot

3.4.2 Boot timing

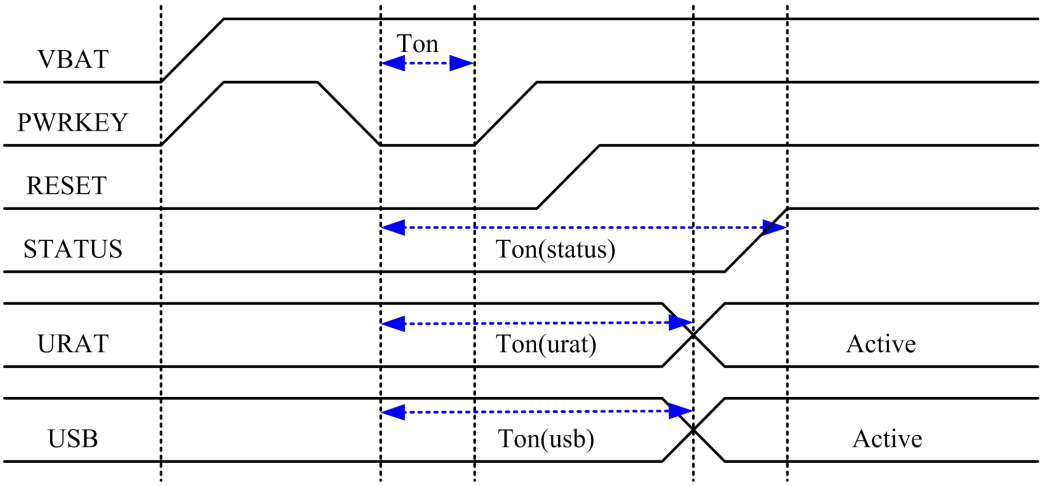


Figure 3-7 Startup timing diagram

Table 3-6 Boot timing parameters

Symbol	Description	Min	Typical	Max	unit
Ton	Boot low level width	100	500	-	ms
Ton(status)	Boot time (according to status status)	22	-	-	ms
Ton(usb)	Boot time (according to usb status)	-	10	-	s
Ton(uart)	Boot time (according to uart status)	-	6	-	s
VIH	PWRKEY input high level	0.6	0.8	1.8	V
VIL	PWRKEY input low level	-0.3	0	0.5	V

It is recommended to use the open-collector drive circuit to control the PWRKEY, which can be released after pulling the base level for 500ms. At this point, the module is powered on. Switching machine design can also be done with buttons, button accessories need to be placed with a TVS tube for ESD protection.

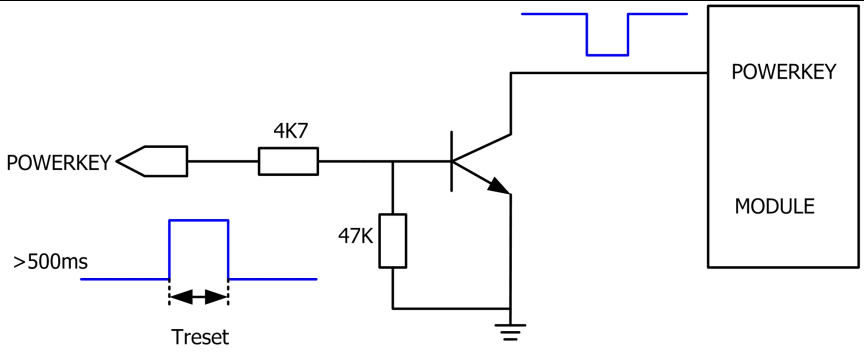


Figure 3-8 Power-on reference circuit

3.4.3 Power down

To shut down the CLM920 TD3 module, the shutdown can be controlled by the PWRKEY pin. At this time, the module performs a normal shutdown process. The module can also be shut down by AT command (this function is under development).

3.4.4 Reset control

The PIN20 signal of the CLM920 TD3 module is the RESET reset pin. When the application detects a module error and the software does not respond, the module can be reset. The module can be reset by pulling the pin low for 100-450ms. The pull-up resistor 10K to VDD_EXT is recommended externally. The RESET pin is sensitive to interference. A 10nF to 0.1uF capacitor can be installed near the signal for signal filtering. Keep away from RF interference signals when routing.

Table 3-7 Reset foot definition

Pin	Signal name	I/O	High value	Description
20	RESET	PI	1.8V±0.3V	Active low

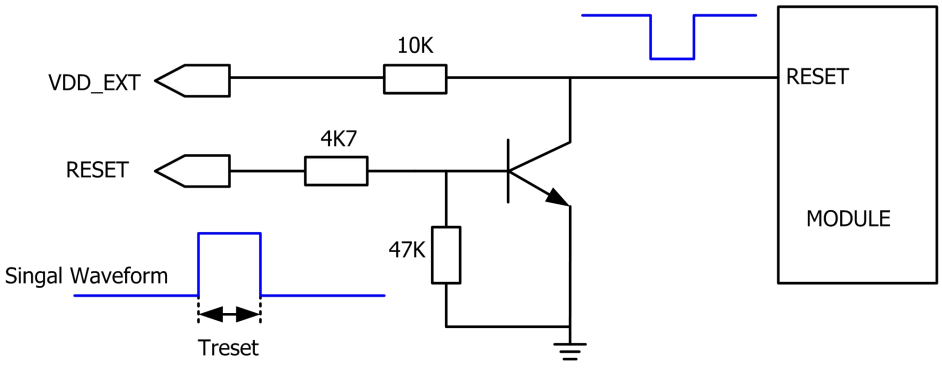


Figure 3-9 Reset reference power

Table 3-8 RESET pin parameters

Symbol	Description	Min	Typical	Max	unit
Treset	Low pulse width	150	200	450	ms
VIH	RESET input high level voltage	1.17	1.8	2.1	V
VIL	RESET input low level voltage	-0.3	0	0.8	V

Reset RESET timing is as follows：

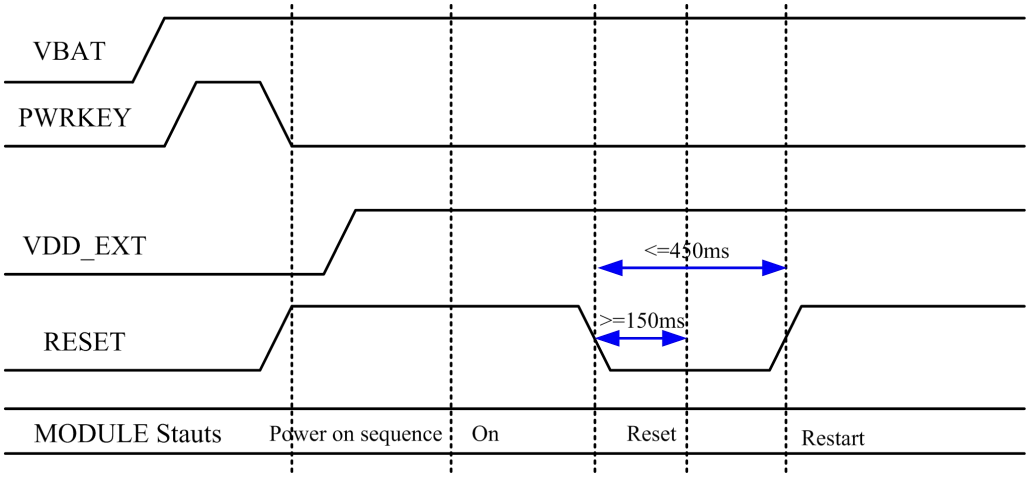


Figure 3-10 Reset timing diagram

The CLM920 TD3 module supports AT command reset, and the AT command is at+cfun=1,1 to restart the module. Detailed instructions for viewing the CLM920 TD3 AT instruction set manual.

3.5 USB interface

The USB interface of the CLM920 TD3 module provides a USB2.0 High-Speed interface. The interface supports slave mode and does not support USB charging mode. USB interface pins are defined as follows：

Table 3-9 USB interface pin definition

Pin number	Signal name	IO	Description
71	USB_VBUS	PI	USB detection
70	USB_DM	IO	USB differential signal -
69	USB_DP	IO	USB differential signal +

The module acts as a USB slave device and supports USB sleep and wake-up mechanisms. USB interface application reference circuit is as follows：

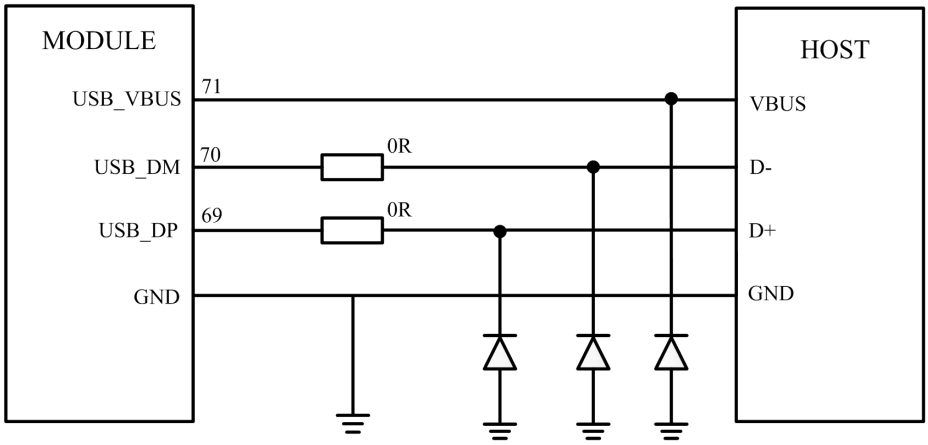


Figure 3-11 USB connection design circuit diagram

NOTE

- The USB interface supports high-speed (480Mbps) and full-speed (12Mbps) modes. Therefore, the trace design needs to strictly follow the USB2.0 protocol requirements. Pay attention to the protection of the data lines, differential traces, and control impedance of 90Ω.
- In order to improve the antistatic performance of the USB interface, it is recommended to add an ESD protection device on the data line. The equivalent capacitance of the protection device is less than 2pF.
- The USB interface bus supply voltage is provided internally by the module and is not required externally. At the same time, since the USB interface of the module does not provide USB bus power, the module can only be used as a slave device of the USB bus device.
- The USB interface can support functions such as software download upgrade, data communication, AT Command, GNSS NMEA output and other functions.

3.6 UART interface

3.6.1 Main serial port

The CLM920 TD3 module provides two sets of UART interfaces. The main serial port and the debug serial port have a serial port level of 1.8V.

Main serial port:

The serial port can realize AT interactive instructions, print program log information, and interact with peripheral data.

The module's serial port baud rate can be set to 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600bps baud rate, the default is 115200bps.

The UART interface is defined as follows：

Table 3-10 UART serial port signal definition

Pin	Signal name	I/O	Description	parameter	Level value (V)			Remarks
					Min	Typical	Max	
62	UART_RI	DO	UART ringing output	VOH	1.35	1.8	2	
				VOL	0		0.45	
63	UART_DCD	DO	UART data carrier detection	VOH	1.35	1.8	2	
				VOL	0		0.45	
64	UART_CTS	DO	UART clear send	VOH	1.35	1.8	2	
				VOL	0		0.45	
65	UART_RTS	DI	Send UART request	VIH	1.2	1.8	2	
				VIL	-0.3		0.6	
66	UART_DTR	DI	UART data is ready	VIH	1.2	1.8	2	
				VIL	-0.3		0.6	
67	UART_TXD	DO	UART send data	VOH	1.35	1.8	2	
				VOL	0		0.45	
68	UART_RXD	DI	UART receive data	VIH	1.2	1.8	2	

When users want to use the full-featured serial port, you can refer to the following connection methods:

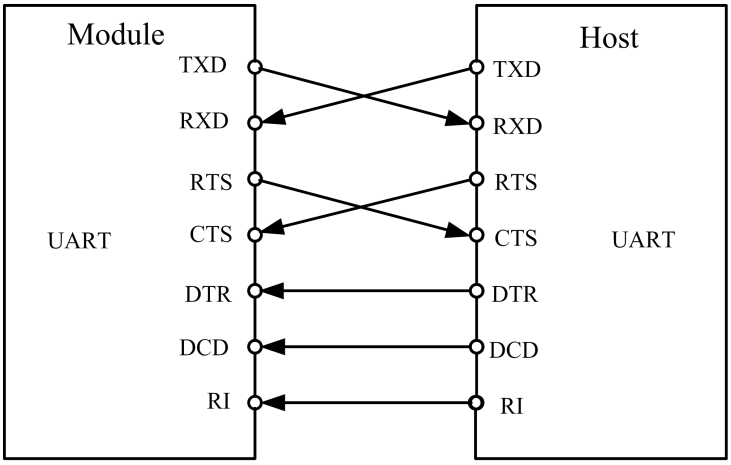


Figure 3-12 Full-featured serial port design

If you need to use a 2-wire serial port, you can refer to the following serial port design.

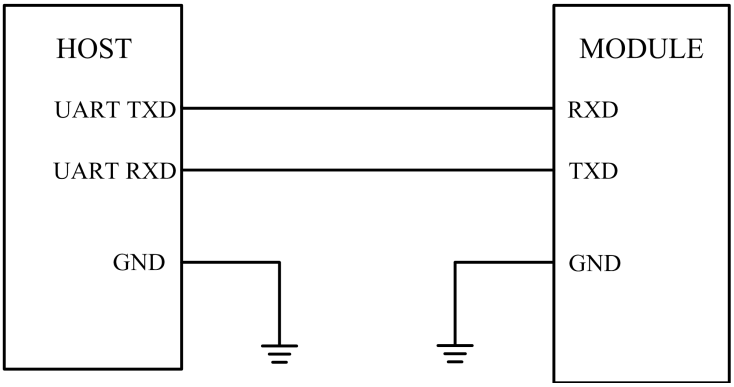


Figure 3-13 UART serial port design

The serial port of the module is TTL 1.8V level. If the serial port needs to be connected to the MCU of 3.3V level, it is necessary to add a level conversion chip externally to achieve level matching. The chip connection method can refer to the following circuit：

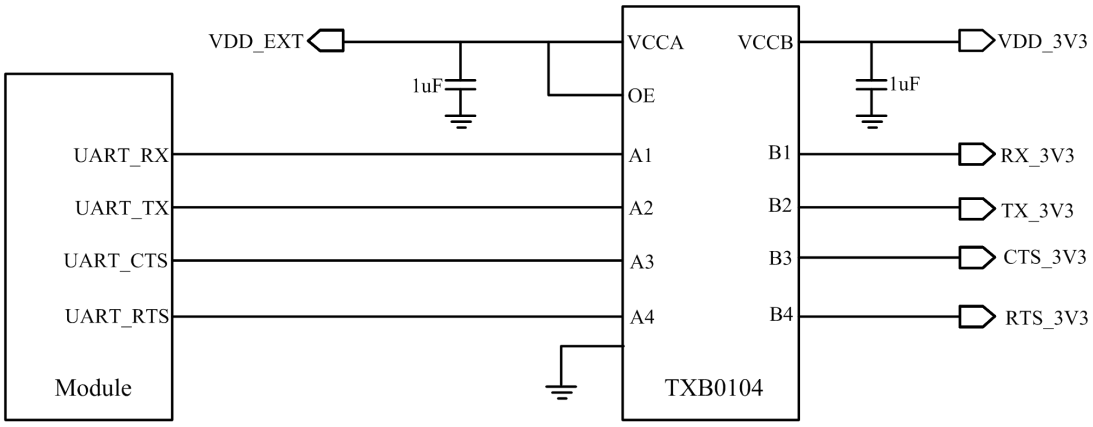


Figure 3-14 Level conversion chip circuit

3.6.2 Debug serial port

The 11th and 12th pins of the module are debug serial port pins, and the debug serial port supports 115200bps baud rate. It is used for Linux control and log printing. It can reserve test points for module debugging. Please do not leave it floating.

Table 3-11 Debugging serial port pin definitions

Pin	Signal name	I/O	Description	Parameter	Level value (V)			Remarks
					Min	Typical	Max	
11	DBG_RXD	DI	UART data reception	VIH	1.2	1.8	2	
				VIL	-0.3		0.6	
12	DBG_TXD	DO	UART data transmission	VOH	1.35	1.8	2	
				VOL	0		0.45	

3.6.3 RI and DTR interface

The CLM920 TD3 module supports the serial sleep wake-up function, and the RI pin can be used as an interrupt to wake up the host.

RI:

The RI pin can wake up the host as an interrupt.

The RI pin idle state is low. When a short message or voice incoming call is received, the RI outputs a rectangular wave with a period of 500ms (high level for 250ms, low level for 250ms) to wake up the host.

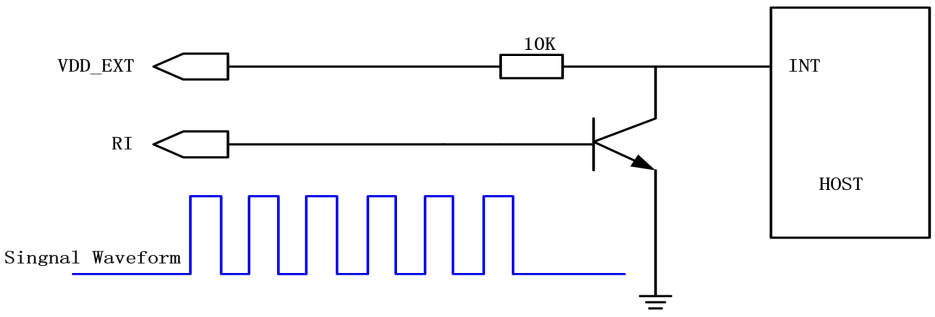


Figure 3-15 RI pin signal waveform

DTR:

The DTR pin can be used as the sleep wake-up pin of the CLM920 TD3 module. When the module enters sleep, the DTR pin can be pulled low to wake up the module.

Pull the DTR pin high first.

Send AT+DISABLEUSB=1, AT+CSCLK=1, and the module will go to sleep.

Pull down the DTR pin wake-up module.

3.7 USIM interface

The CLM920 TD3 module provides a USIM card interface compatible with the ISO 7816-3 standard. The USIM card power supply is provided by the module's internal power manager and supports 1.8V/3.0V voltage.

Table 3-12 SIM card signal definition

Pin	Signal name	I/O	Description	Parameter	Level value (V)			Remarks
					Min	Typical	Max	
13	USIM_DET	DI	USIM card detection	VIH	1.6	1.8	2	This pin signal is internally pulled high. If the USIM_DET pin is not used, leave it floating.
				VIL	0		0.18	
14	USIM_VDD	PO	USIM card power supply	V3.0	2.75	3.0	3.05	USIM_VDD=3.0V
				V1.8	1.75	1.8	1.95	
15	USIM_DATA	IO	USIM card data	VIH	0.65*VDD		3.05	USIM_VDD=1.8V
				VIL	-0.3	0	0.25*VDD	
				VOH	VDD-0.45		3.05	
				VOL	0	0	0.45	
16	USIM_CLK	DO	USIM card clock	VOH	VDD-0.45		3.05	USIM_VDD:3.0V/1.8V
				VOL	0	0	0.45	
17	USIM_RST	DO	USIM card	VOH	VDD-0.45		3.05	USIM_VDD:3.0V/1.8V

			reset	VOL	0	0	0.45	

3.7.1 USIM card reference circuit

The CLM920 TD3 module does not come with a USIM card slot. Users need to design a USIM card slot on their own interface board. USIM card interface reference circuit is as follows：

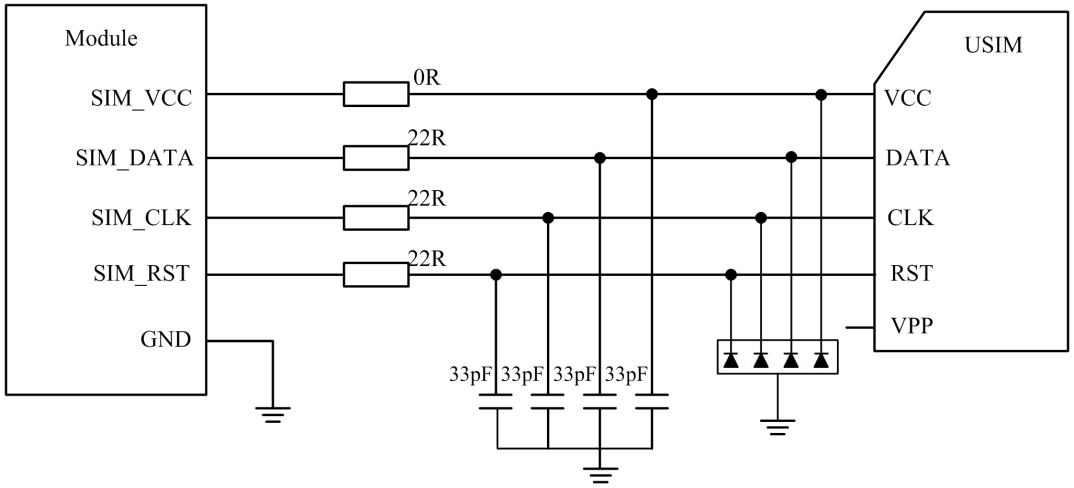


Figure 3-16 USIM design circuit diagram

NOTE

- ✧ It is recommended to select ONSEMI's SMF15C device for ESD protection on the SIM interface line. The peripheral circuit device should be placed close to the card holder, and the SIM card holder is close to the module layout.
- ✧ The USIM card circuit is susceptible to radio frequency interference and does not recognize or drop the card. Therefore, the card slot should be placed as far as possible from the RF radiation of the antenna. The card trace should be as far away as possible from the RF, power supply and high-speed signal lines.
- ✧ The UIM_DATA has been internally pulled up to VDD_EXT through a 47K resistor, and no external pull-up is required.
- ✧ UIM_DET is the USIM card insertion or non-insertion detection pin. It is high by default. The SIM card status can be detected by this PIN pin during hot plug application.
- ✧ To avoid transient voltage overload, the USIM interface requires a 22R resistor in series with each other on the signal line path.
- ✧ The ground of the USIM deck and the ground of the module should maintain good connectivity.

3.7.2 UIM_DET Hot Swap Reference Design

The CLM920 TD3 module supports the USIM card hot plug function. The UIM_DET pin acts as an input detection pin to determine whether the USIM card is inserted or not. The UIM_DET pin defaults to a pull-up high. The hot plug function can be turned on or off by AT+HOSCFG. This function is off by default (see the 9X07 AT command set for details).

Table 3-13 SIM card hot swap detection pin definition

NO.	AT command	UIM_DET status	Functional description
1	AT+HOSCFG=1,1	high	SIM card insertion, UIM_DET is high
2	AT+HOSCFG=1,0	low	SIM card insertion, UIM_DET is low

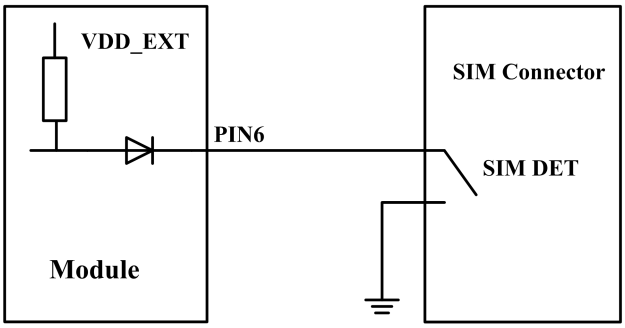


Figure 3-17 Hot swap detection of the USIM card

NOTE

- ✧ It is recommended to add a diode protection next to the UIM_DET pin of the module.
- ✧ When using a normally closed SIM card holder or a normally open SIM card holder, the detection function can be set by the AT command. If AT+HOSCFG=1 is set, the status of the SIM card is high when the SIM card is in position, and AT+HOSCFG=1 is set. When the SIM card is in the state, the status is low. Set AT+HOSCFG=0, 0 SIM card hot swap function is off.

3.8 General purpose GPIO interface

The CLM920 TD3 module contains five general control signals. The interface is defined as follows：

Table 3-14 General GPIO Pin Definitions

Pin	Signal name	I/O	Description	parameter	Level value (V)			Remarks
					Min	Typical	Max	

1	WAKEUP_IN	DI	Sleep mode control	VIH	1.2	1.8	2	
				VIL	-0.3		0.6	
2	AP_READY	DI	Sleep state detection	VIH	1.2	1.8	2	This feature is under development
				VIL	-0.3		0.6	
3	GPIO_1	IO	This pin function has not been defined					RESERVE, please keep it floating
4	W_DISABLE#	DI	Flight mode control	VIH	1.2	1.8	2	This feature is under development
				VIL	-0.3		0.6	
5	GPIO_2	IO	This pin function has not been defined					RESERVE, please keep it floating

WAKEUP_IN:

This pin is the host wake-up module pin. When the WAKEUP_IN signal is pulled low, the host can wake up the module.

AP_READY (this feature is under development)

The AP_READY pin can be used by the module to detect if the host is woken up and can be configured for high level detection or low level detection.

W_DISABLE#:

Flight mode control (this function is under development), when the CLM920 TD3 module W_DISABLE# signal is pulled low, the module RF function can be turned off, the module can enter the flight mode, and the module can be turned on to open the module RF function. It can also be set to flight mode by AT+CFUN. For details, please refer to CLM920 TD3 AT command set.

3.9 Network status indication interface

The CLM920 TD3 module provides an open-drain GPIO signal to indicate RF communication status.

Table 3-15 Network indicator pin definition

Pin	Signal name	I/O	Description
6	NET_STATUS	OD	Network status indication

Table 3-16 Network indication status

status	LED display status
No service	Constantly bright
Module registration on non-4G network	Slow flash
The module registers 4G network or module to register non-4G network for voice SMS and other services.	Flashing

LED network indicator reference design is as follows：

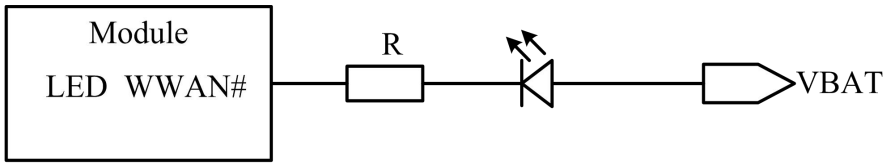


Figure 3-18 Network indicator circuit diagram

NOTE

✧ The brightness of the network indicator can be adjusted by adjusting the current limiting resistor R. The current can be adjusted up to 40mA.

3.10 Module status indication

The CLM920 TD3 module provides a pin as a working status indicator of the module. This pin can be used to connect to a GPIO or LED with pull-up. It is used to indicate the power-on status of the module. The drive current should be less than 0.8mA. , STATUS pin will output low level, and the rest will be high impedance state.

Table 3-17 Module Status Pin Definitions

Pin	Signal name	I/O	Description	Remarks
61	STATUS	DO	Module power on status indication	External pull-up

The following figure shows the STATUS reference circuit design:

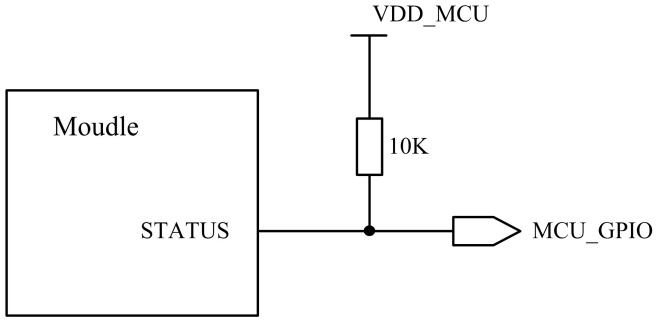


Figure 3-19 STATUS Pin Reference Circuit

3.11 PCM digital voice interface

The CLM920 TD3 module provides a set of PCM audio interfaces supporting 8-bit A-rate, U-rate and 16-bit linear short frame encoding formats with PCM_SYNC of 8kHZ and PCM_CLK of 2048kHZ.

Table 3-18 PCM pin definition

Pin	Signal name	I/O	Description	Para meter	Level value (V)			Rem arks
					Min	Typical	Max	
24	PCM_IN	DI	PCM data input	VIH	1.2	1.8	2	
				VIL	-0.3		0.6	
25	PCM_OUT	DO	PCM data output	VOH	1.35	1.8	2	
				VOL	0		0.45	
26	PCM_SYNC	DO	PCM frame sync signal	VOH	1.35	1.8	2	
				VOL	0		0.45	
27	PCM_CLK	DO	PCM clock pulse	VOH	1.35	1.8	2	
				VOL	0		0.45	

Table 3-19 PCM specific parameters

Characteristic	Description
Encoding format	Linear
Data bit	16bits
Master-slave mode	Master/slave mode
PCM clock	2048kHz
PCM frame synchronization	Short frame

Data Format	MSB

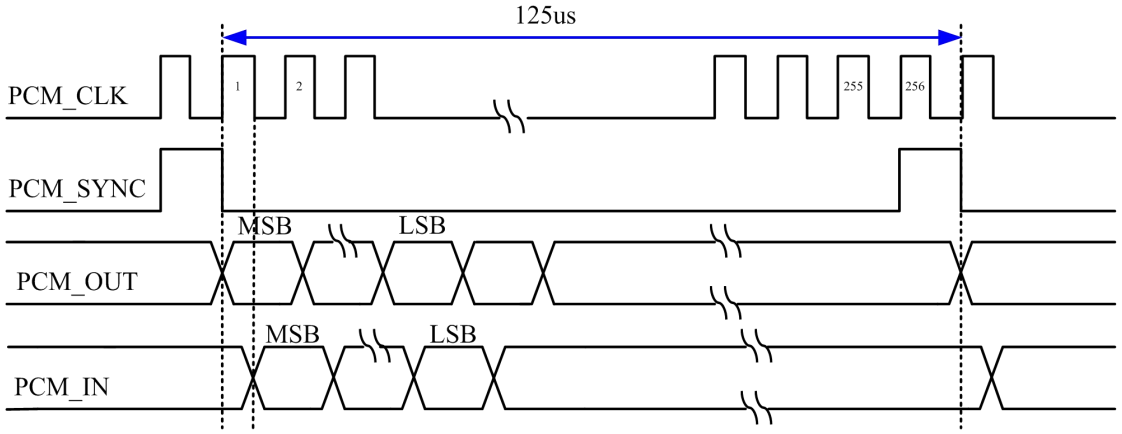


Figure 3-20 PCM short frame mode timing diagram

PCM to analog voice recommendation circuit is as follows：

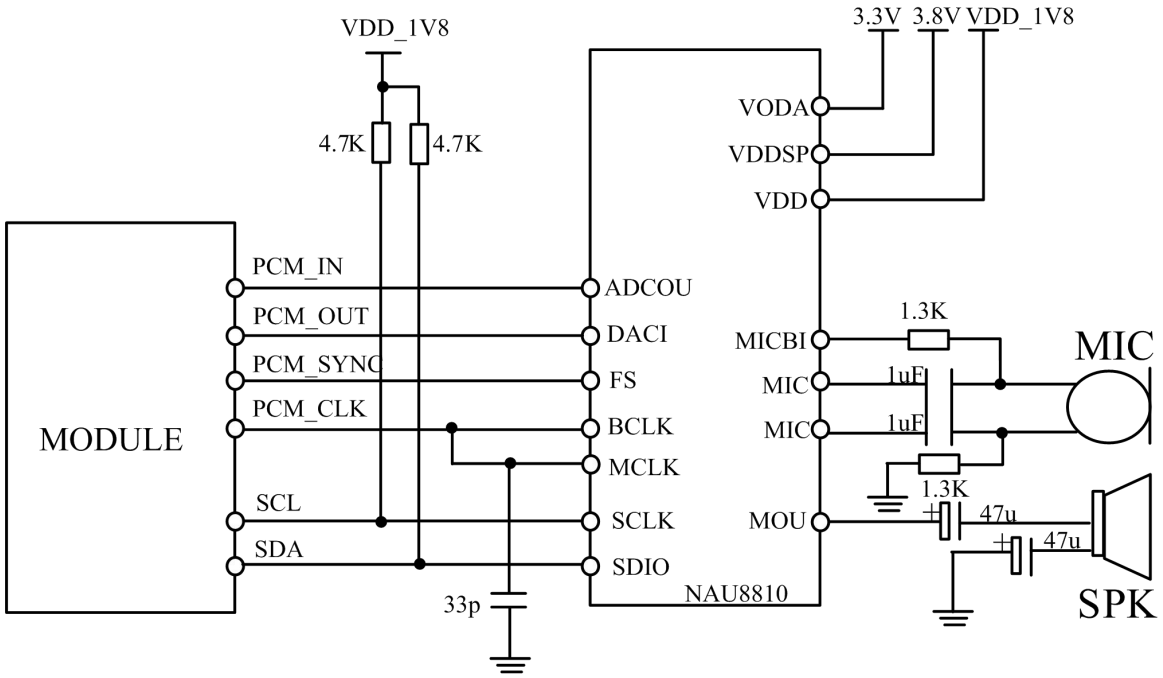


Figure 3-21 PCM to analog voice map

3.12 I2C bus

CLM920 TD3 module provides a set of hardware bidirectional serial bus, I2C interface is 1.8V level, 5.0 protocol interface, clock rate is 400KHz.

Table 3-20 I2C pin definition

Pin	Signal	I/O	Description	Para	Level value (V)	Rema

	name			meter	Min	Typical	Max	rks
41	I2C_SCL	DO	I2C bus clock output	VOH	1.35	1.8	2	
				VOL	0		0.45	
42	I2C_SDA	IO	I2C bus data input and output	VOH	1.35	1.8	2	
				VOL	0		0.45	
				VIH	1.2	1.8	2	
				VIL	-0.3		0.6	

I2C reference circuit connection is as follows：

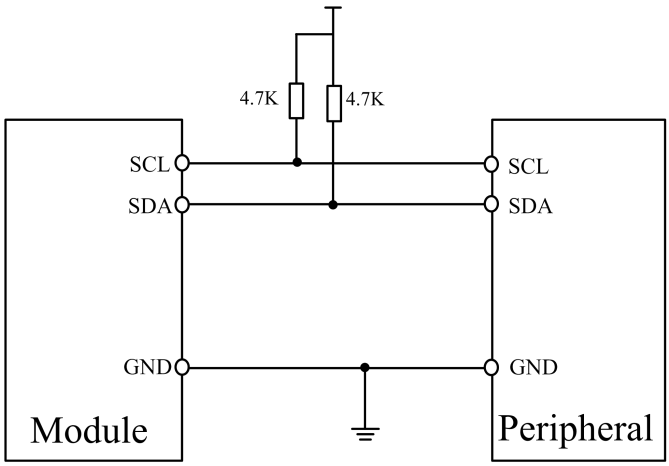


Figure 3-22 I2C interface reference circuit diagram

3.13 SDIO interface

CLM920 TD3 module provides one 4-bit SD/MMC interface, supports 1.8V/2.95V two voltage SD cards, clock frequency up to 50MHz, maximum capacity support 32GB, support SD3.0 protocol.

Table 3-21 SD card pin definition

Pin	Signal name	I/O	Description	Parameter	Level value (V)			Remarks
					Min	Typical	Max	
23	SD_CARD_DET	DI	SD card insertion detection	VIH	1.2	1.8	2	
				VIL	-0.3		0.6	
28	SDC2_D3	IO	SDIO bus DATA3	VOH	1.35	1.8	2	1.8V voltage domain

				VOL	0		0.45	1.8V voltage domain
				VIH	1.27	1.8	2	1.8V voltage domain
				VIL	-0.3		0.6	1.8V voltage domain
				VOH	0.75* VDD_Px	2.95	VDD_Px	2.95V voltage domain
				VOL	0		0.125* VDD_Px	2.95V voltage domain
				VIH	0.625* VDD_Px	2.95	VDD_Px + 0.3	2.95V voltage domain
				VIL	-0.3		0.25* VDD_Px	2.95V voltage domain
29	SDC2_D2	IO	SDIO bus DATA2	VOH	1.35	1.8	2	2.95V voltage domain
				VOL	0		0.45	1.8V voltage domain
				VIH	1.27	1.8	2	1.8V voltage domain
				VIL	-0.3		0.6	1.8V voltage domain
				VOH	0.75* VDD_Px	2.95	VDD_Px	2.95V voltage domain
				VOL	0		0.125* VDD_Px	2.95V voltage domain
				VIH	0.625* VDD_Px	2.95	VDD_Px + 0.3	2.95V voltage domain
				VIL	-0.3		0.25* VDD_Px	2.95V voltage domain
30	SDC2_D1	IO	SDIO bus DATA1	VOH	1.35	1.8	2	1.8V voltage domain
				VOL	0		0.45	1.8V voltage

								domain
				VIH	1.27	1.8	2	1.8V voltage domain
				VIL	-0.3		0.6	1.8V voltage domain
				VOH	0.75* VDD_Px	2.95	VDD_Px	2.95V voltage domain
				VOL	0		0.125* VDD_Px	2.95V voltage domain
				VIH	0.625* VDD_Px	2.95	VDD_Px + 0.3	2.95V voltage domain
				VIL	-0.3		0.25* VDD_Px	2.95V voltage domain
31	SDC2_ D0	IO	SDIO bus DATA0	VOH	1.35	1.8	2	1.8V voltage domain
				VOL	0		0.45	1.8V voltage domain
				VIH	1.27	1.8	2	1.8V voltage domain
				VIL	-0.3		0.6	1.8V voltage domain
				VOH	0.75* VDD_Px	2.95	VDD_Px	1.8V voltage domain
				VOL	0		0.125* VDD_Px	2.95V voltage domain
				VIH	0.625* VDD_Px	2.95	VDD_Px + 0.3	2.95V voltage domain
				VIL	-0.3		0.25* VDD_Px	2.95V voltage domain
32	SDC2_ CLK	DO	SDIO Bus clock	VOH	1.35	1.8	2	1.8V voltage domain
				VOL	0		0.45	1.8V voltage domain

				VOH	0.75* VDD_Px	2.95	VDD_Px	2.95V voltage domain
				VOL	0		0.125* VDD_Px	2.95V voltage domain
33	SDC2_ CMD	IO	SDIO bus command	VOH	1.35	1.8	2	1.8V voltage domain
				VOL	0		0.45	1.8V voltage domain
				VIH	1.27	1.8	2	1.8V voltage domain
				VIL	-0.3		0.6	1.8V voltage domain
				VOH	0.75* VDD_Px	2.95	VDD_Px	2.95V voltage domain
				VOL	0		0.125* VDD_Px	2.95V voltage domain
				VIH	0.625* VDD_Px	2.95	VDD_Px + 0.3	2.95V voltage domain
				VIL	-0.3		0.25* VDD_Px	2.95V voltage domain
34	VDD_ SDIO	PO	SDIO bus pull-up power supply	IO maximum output 50MA, output 1.8V/2.85V configurable				Cannot be used for SD card power supply

The SD card reference design of the CLM920 TD3 module is shown in the figure below：

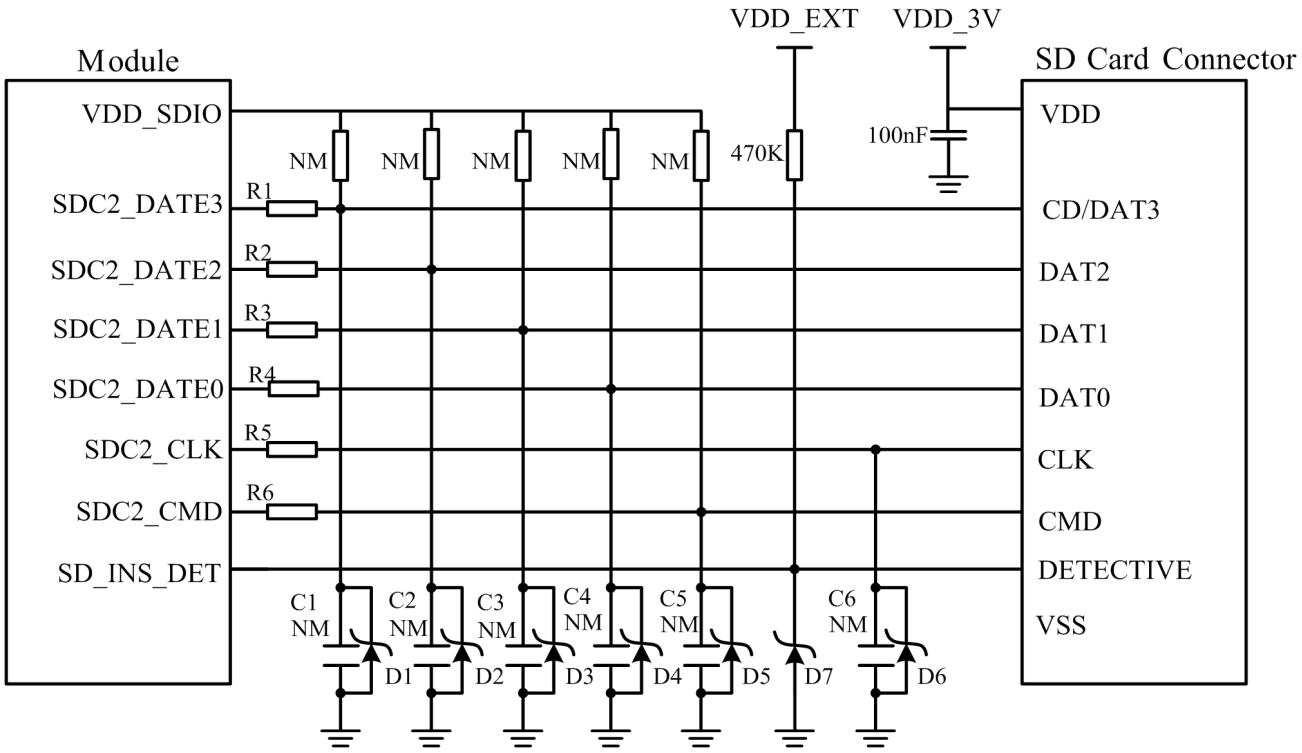


Figure 3-23 SD card interface reference circuit diagram

NOTE

SD card circuit wiring notes:

- ✧ The SD card power supply has a 3V voltage range of 2.7~3.6V and needs to be externally supplied with a minimum current of 800mA.
- ✧ The maximum output current of the module output power VDD_SDIO is 50mA, which can only be used for SDIO bus pull-up.
- ✧ The clock frequency of the SD card is as high as 200 MHZ, and the trace is preferably controlled by 50 ohm impedance.
- ✧ The length of the signal line should be less than 25mm. The spacing of the signal lines should be 2 times the line width and cover the ground and keep away from other possible interference.
- ✧ The spacing between the SDIO signal and other signals needs to be greater than 2 line widths and ensure that the bus load is less than 40pF.
- ✧ The pull-up resistor is added to the SDIO signal, the resistance range is 10~100kΩ, the recommended value is 100kΩ, and it is pulled up to the VDD_SDIO pin of the module.
- ✧ In order to ensure good ESD performance, it is recommended to add TVS tube to the SD card pin and place it near the pin.

3.14 SPI interface / multiplexed I2S interface

The CLM920 TD3 provides an SPI interface with a maximum clock rate of 50MHz. In addition, the module can only be used as the master, and the interface voltage domain is 1.8V.

Table 3-22 SPI Pin Definitions

Pin	Signal name	I/O	Description	Parameter	Level value (V)			Remarks
					Min	Typical	Max	
37	SPI_CS_N	DO	SPI chip selection	VOH	1.35	1.8	2	Multiplexing I2S_D1
				VOL	0		0.45	
38	SPI_MOSI	DO	SPI data output	VOH	1.35	1.8	2	Reuse I2S_WS
				VOL	0		0.45	
39	SPI_MISO	DI	SPIO data input	VIH	1.2	1.8	2	Multiplexing I2S_D0
				VIL	-0.3		0.6	
40	SPI_CLK	DO	SPI clock	VOH	1.35	1.8	2	Multiplexing I2S_CLK
				VOL	0		0.45	

The SPI interface of the CLM920 TD3 module can also be used as I2S. It can be connected to the CODEC. The existing I2S supports the Nuvoton NAU8810 by default.

Table 3-23 I2S pin definition

Pin	Signal name	I/O	Description	Parameter	Level value (V)			Remarks
					Min	Typical	Max	
37	I2S_D1	IO	I2S serial data	VOH	1.35	1.8	2	
				VOL	0		0.45	
				VIH	1.2	1.8	2	
				VIL	-0.3		0.6	
38	I2S_WS	IO	I2S command selection	VOH	1.35	1.8	2	
				VOL	0		0.45	
				VIH	1.2	1.8	2	
				VIL	-0.3		0.6	
39	I2S_D0	IO	I2S serial data	VOH	1.35	1.8	2	
				VOL	0		0.45	
				VIH	1.2	1.8	2	
				VIL	-0.3		0.6	

40	I2S_CLK	IO	I2S clock	VOH	1.35	1.8	2	
				VOL	0		0.45	
				VIH	1.2	1.8	2	
				VIL	-0.3		0.6	

The following figure shows the reference design of the CLM920 TD3 connected to the NAU8810:

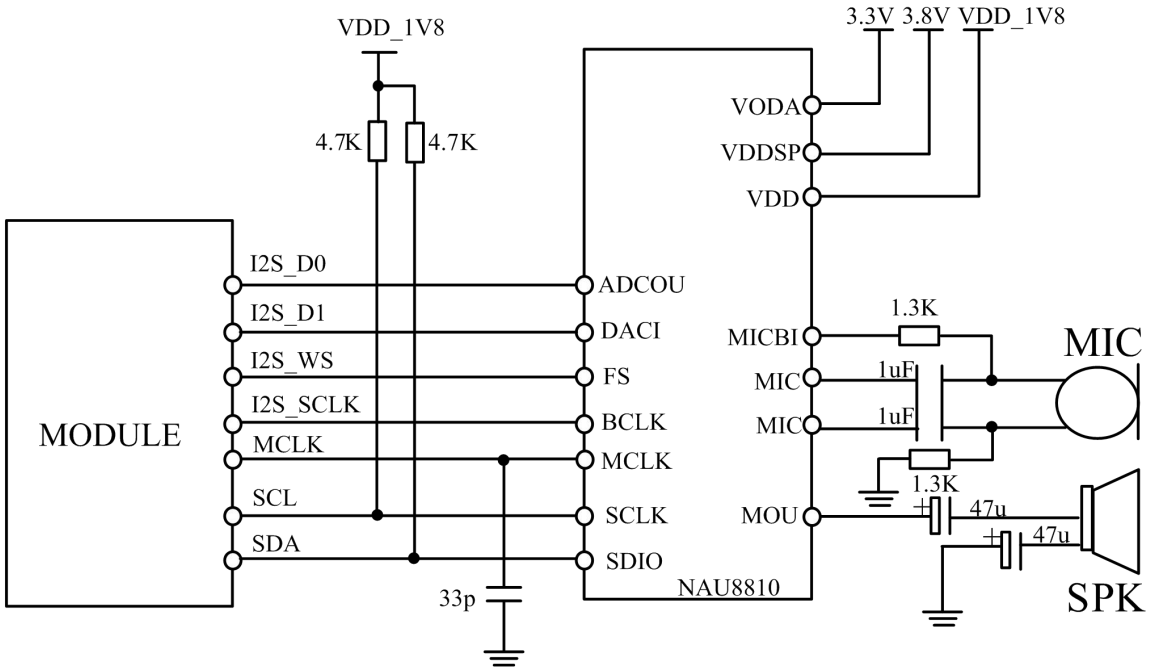


Figure 3-24 I2S to analog voice map

3.15 MCLK interface

The CLM920 TD3 module provides one MCLK and provides a 12.288M clock output. This interface is mainly used to connect the MCLK of the CODEC chip. The main clock frequency of the NAU8810 is supported by default.

Table 3-24 MCLK Pin Definitions

Pin	Signal name	I/O	Description	Parameter	Level value (V)			Remarks
					Min	Typical	Max	
116	MCLK	D0	I2S master clock	VOH	1.35	1.8	2	The default output is 12.288M
				VOL	0		0.45	

3.16 WLAN interface

CLM920 TD3 module provides low power SDIO 3.0 interface for WLAN design.

Table 3-25 WLAN pin definitions

Pin	Signal name	Description	I/O	Remarks
127	PM_ENABLE	Power enable	DO	Keep empty when not in use
129	SDC1_DATA3	Data bus DATA3	IO	Keep empty when not in use
130	SDC1_DATA2	Data bus DATA2	IO	Keep empty when not in use
131	SDC1_DATA1	Data bus DATA1	IO	Keep empty when not in use
132	SDC1_DATA0	Data bus DATA0	IO	Keep empty when not in use
133	SDC1_CLK	WLAN clock	DO	Keep empty when not in use
134	SDC1_CMD	WLAN command	IO	Keep empty when not in use
136	WLAN_EN	WLAN enable	DO	Keep empty when not in use
118	WLAN_SLP_CLK	WLAN sleep clock	DO	Keep empty when not in use
135	WAKE_WLAN	WLAN wake-up module	DI	Keep empty when not in use
137	COEX_UART_RXD	WLAN coexistence reception	DI	Keep empty when not in use
138	COEX_UART_TXD	WLAN coexistence transmission	DO	Keep empty when not in use

NOTE

- ✧ For the interface multiplexing function, please refer to the corresponding function chapter.
- ✧ When using WLAN, the coexisting serial port needs to be used at the same time. Coexisting serial port cannot be used as a normal serial port.

CLM920 TD3 module wireless connection interface and YG30 reference design as shown below：

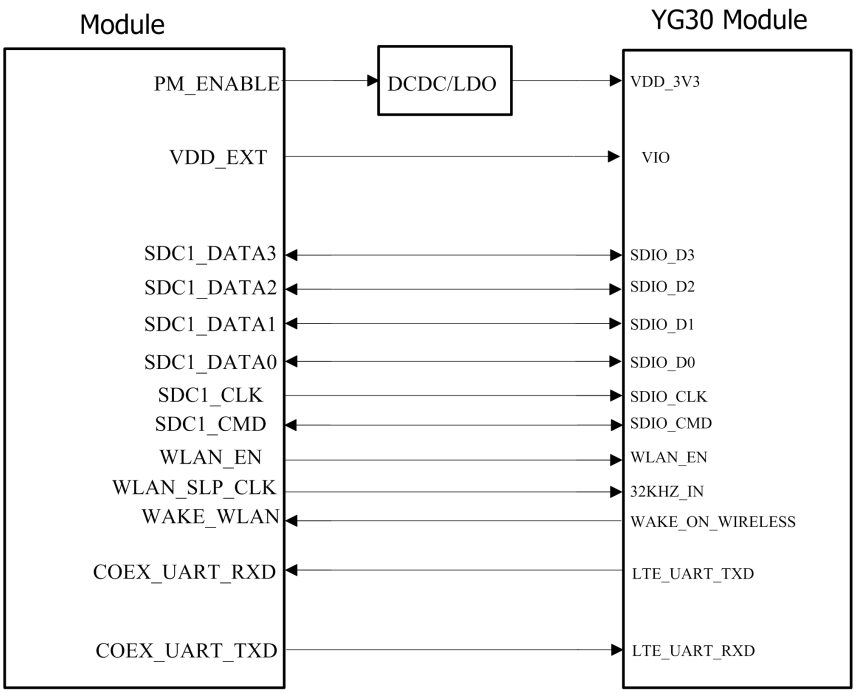


Figure 3-25 Wireless connection interface and YG30 reference design

The SDIO interface supports single rate mode with a maximum frequency of 50MHz. The SDIO interface has a high rate. To ensure that the interface design conforms to the SDIO 3.0 specification, the following guidelines are recommended:

✧ The SDIO signal line requires a three-dimensional package and the impedance needs to be controlled at 50Ω ± 10%.

✧ SDIO signal lines need to be away from sensitive signals such as RF, analog signals, and noise signals such as clocks and DCDCs.

✧ The SDC1_CLK signal line needs to be placed close to the module to place 15Ω~24Ω termination matching resistor; the SDC1_CLK pin to resistor should be less than 5mm.

✧ The spacing between the SDIO signal and other signals needs to be greater than 2 line widths and ensure that the bus load is less than 15pF.

✧ SDC1_CLK and SDC1_DATA[0:3]/SDC1_CMD need to be treated as equal length (with a difference of less than 1mm), and the total length should be less than 50mm.

3.17 SGMII interface

The CLM920 TD3 module provides an SGMII interface with embedded Ethernet MAC and a two-wire management interface. The key features are as follows:

✧ Comply with the IEEE 802.3 standard.

✧ Support 10/100/1000M working mode.

✧ The maximum downlink rate is 150Mbs and the maximum uplink rate is 50Mbs (in 4G network).

✧ Support for VLAN tagging.

✧ Supports 3EEE 1588 and PTP protocols.

✧ Can be connected to an external Ethernet PHY chip such as the AR8033, or an external switch.

✧ Management interface supports 1.8V/2.85V dual voltage.

The SGMII interface pin is defined as follows：

Table 3-26 SGMII interface pin definition

Pin	Signal name	Description	IO	Remarks
119	EPHY_RST_N	Ethernet PHY reset	DO	1.8V/2.85 voltage domain
120	EPH_INT_N	Ethernet PHY interrupt	DI	1.8 voltage domain
121	SGMII_MDATA	SGMII MDIO data	IO	1.8V/2.85 voltage domain
122	SGMII_MCLK	SGMII MDIO clock	DO	1.8V/2.85 voltage domain
128	USIM2_VDD	SGMII_MDATA pull-up power supply	PO	1.8V/2.85 voltage domain
123	SGMII_TX_M	SGMII differential data transmission negative signal	AO	0.1 μ F capacitor in series near the chip end
124	SGMII_TX_P	SGMII differential data transmission positive signal	AO	Connect 0.1 μ F capacitor in series near the chip end
125	SGMII_RX_P	SGMII differential data receiving positive signal	AI	Connect 0.1 μ F capacitor in series near the module end
126	SGMII_RX_M	SGMII differential data receiving negative signal	AI	Connect 0.1 μ F capacitor in series near the module end

Ethernet application plan:

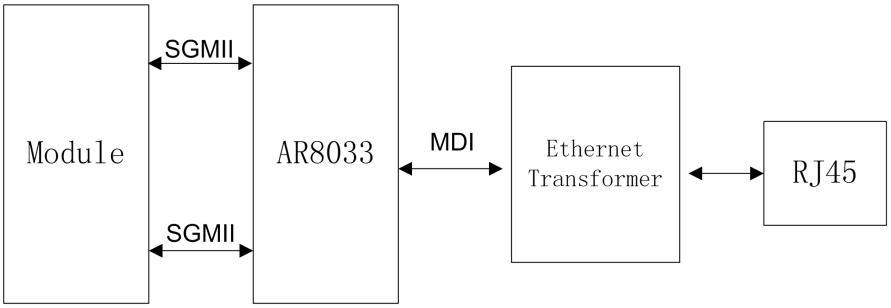


Figure 3-26 Schematic diagram of the Ethernet application solution

CLM920 TD3 module SGMII interface and Ethernet PHY chip AR8033 reference design as shown below:

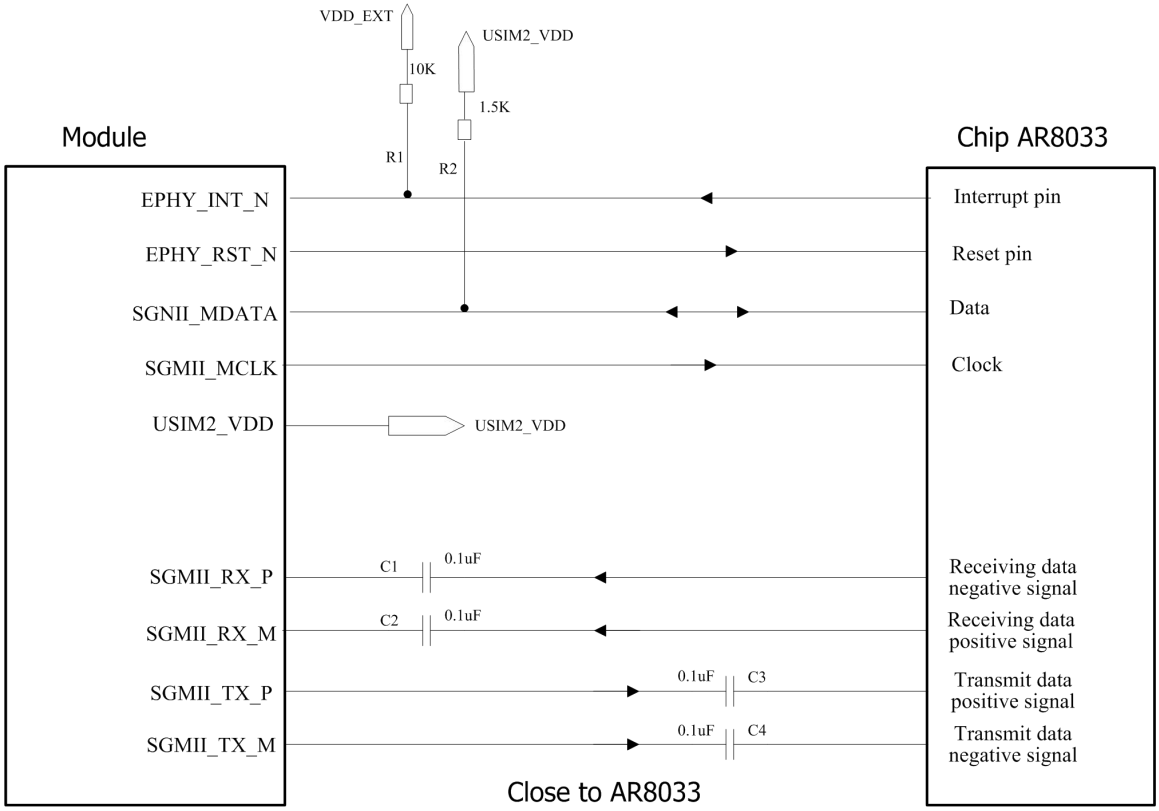


Figure 3-27 SGMII interface and Ethernet PHY core AR8033 reference design

3.18 ADC interface

The CLM920 TD3 provides two analog-to-digital converter interfaces to read the voltage value. The input voltage of the ADC interface cannot exceed VBAT. It is recommended that the ADC pin be input with a voltage divider circuit.

Table 3-27 ADC Pin Definitions

Pin	Signal name	Description	para meter	Level value (V)			Remarks
				Min	Typical	Max	
44	ADC1	Analog to digital converter interface 0	VIN	0.3		VBAT	ADC resolution 15Bits
45	ADCO	Analog to digital converter interface 0	VIN	0.3		VBAT	ADC resolution 15Bits

3.19 RF interface

CLM920 TD3 module provides three-way antenna interface, one main set antenna interface, responsible for 4G, 3G, 2G signals of transceiver module, one-way diversity antenna interface, responsible for receiving 4G, 3G signals, and signal degradation caused by multi-path under high-speed movement The signal can be enhanced by adding a diversity antenna, and a GNSS antenna interface is used for GPS, Beidou, GLONASS, and GALILEO signal reception, and can provide a positioning solution for the user. Three-way antenna interface impedance is 50 ohms.

Table 3-28 Antenna interface pin definition

Pin	Signal name	I/O	Description	Remarks
49	ANT_MAIN	IO	Main antenna interface	50Ω characteristic impedance
35	ANT_DIV	AI	Diversity antenna interface	50Ω characteristic impedance
47	ANT_GNSS	AI	GNSS antenna interface	50Ω characteristic impedance

3.19.1 Main antenna interface

The 49-pin of the CLM920 TD3 is the main set antenna interface. To facilitate the debugging of the antenna, it is necessary to add a π-type matching circuit to the motherboard, and take the 50-ohm impedance line. The recommended circuit is as follows：

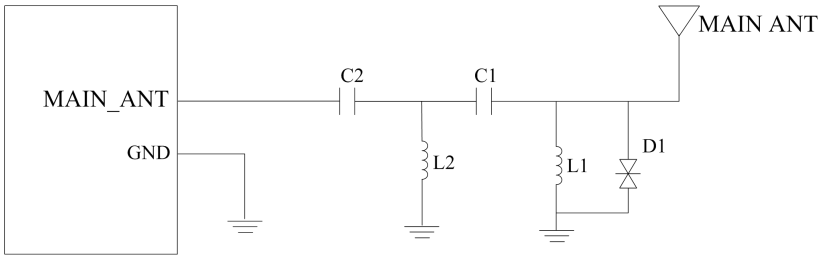


Figure 3-28 Main antenna matching circuit

3.19.2 Diversity antenna interface

The 35-pin of the CLM920 TD3 is a diversity antenna interface. To facilitate antenna debugging, a π-type matching circuit needs to be added to the main board, and a 50-ohm impedance line is required. The main antenna and the diversity antenna need to maintain a certain spacing. The recommended circuit is as shown below：

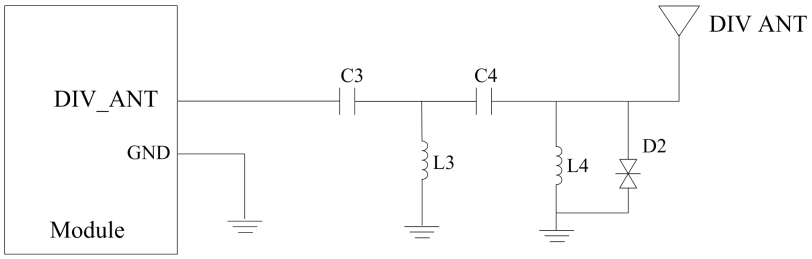


Figure 3-29 Diversity Antenna Matching Circuit

3.19.3 GNSS interface

The 47 pin of the CLM920 TD3 is a GNSS antenna interface. It supports GPS, BEIDOU, GLONASS, and GALILEO signal reception. If you need to use it, you need to use the AT command AT+CGPS=1 to turn on the GPS (for details, please refer to the CLM920 TD3 AT command set manual) In order to facilitate the debugging of the antenna, it is necessary to add a π-type matching circuit to the main board, and take a 50-ohm impedance line. The GNSS antenna needs to maintain a certain distance from the main antenna and the diversity antenna. The GNSS antenna has two antenna connection modes, and the other is a connection. Passive antenna, the other is to connect the active antenna. Since the module itself cannot supply power to the GNSS active antenna, it needs to be externally provided. The recommended circuit is as shown below：

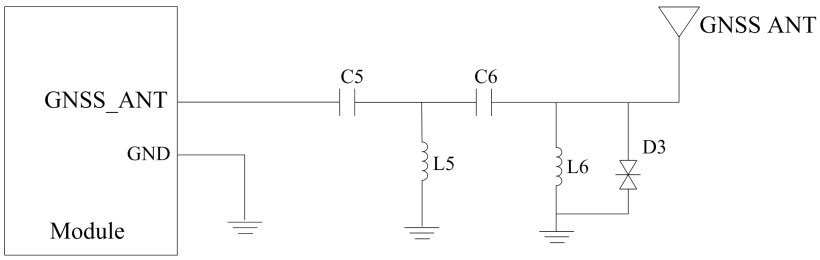


Figure 3-30 GNSS passive antenna reference circuit

The figure below shows L5 in the active antenna matching circuit. L6 is not attached by default. C5 is affixed to 100pF by default. The specific value is provided by the antenna factory after the antenna is debugged. C6 defaults to 100pF, which is a DC blocking capacitor.

Active antenna power supply VDD needs to match the active antenna of the application, and it is recommended that customers use LDO/DCDC to power the active antenna, so that when the GNSS function is not used, the LDO/DCDC can be turned off to reduce the current consumption.

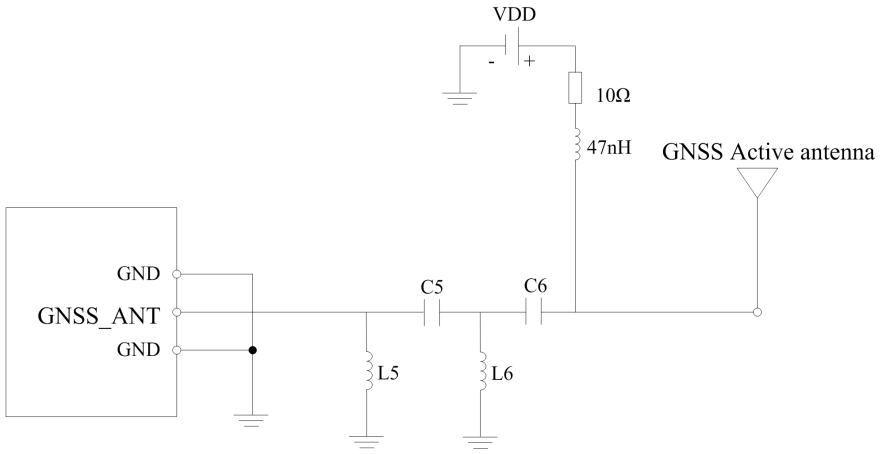


Figure 3-31 GNSS active antenna reference circuit

NOTE

- ✧ The CLM920 TD3 module provides three RF antenna interfaces, which are the main set antenna, the diversity antenna and the GPS antenna connection port. The antenna interface must be a 50 ohm characteristic impedance trace.
- ✧ In actual use, according to the user's circuit board routing, the antenna factory debugs and optimizes the matching device parameter values. The motherboard C1/C2/C3/C4/C5/C6 defaults to 100pF, L1/L2/L3/L4/L5/L6 defaults to empty. In order to prevent static damage to the internal part of the module, it is recommended to attach a bidirectional TVS tube at the antenna connection D1/D2/D3.
- ✧ The parasitic capacitance of the TVS tube pins themselves must be small to avoid signal interference. The ESD protection component used on the antenna must take into account the frequency band used by the antenna and the minimum parasitic capacitance that can be accepted by different frequency bands. The ESD protection component usually used on the antenna must have a parasitic capacitance value of less than 0.5pF or even more. low.
- ✧ Antenna impedance traces need to be away from digital signal lines, power supplies and other interference signals.

✧ The antenna impedance traces need to be three-dimensionally packaged, and the ground holes are added on both sides of the trace to isolate.

3.19.4 RF trace reference

For the user, the characteristic impedance of all RF signal lines should be controlled at 50Ω. The impedance of the RF signal line is determined by the dielectric constant of the material, the trace width (W), the ground clearance (S), and the height of the reference ground plane (H). Please use the impedance simulation tool to calculate the impedance value of the RF trace. The control of the PCB characteristic impedance is usually in the form of microstrip lines and coplanar waveguides.

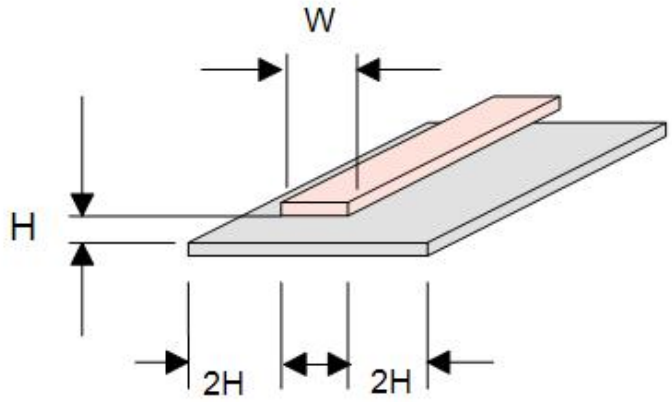


Figure 3-32 The complete structure of the two-layer PCB microstrip line

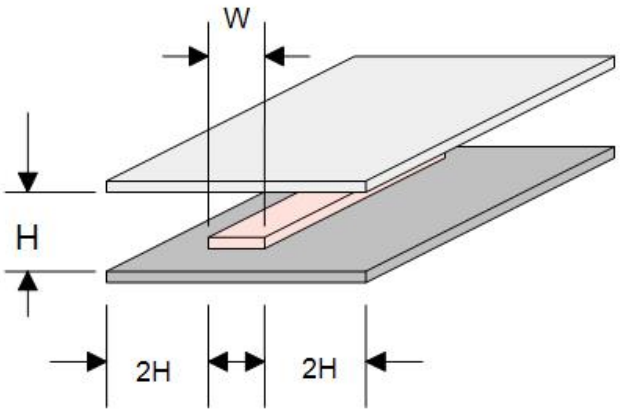


Figure 3-33 The complete structure of the multilayer PCB strip line

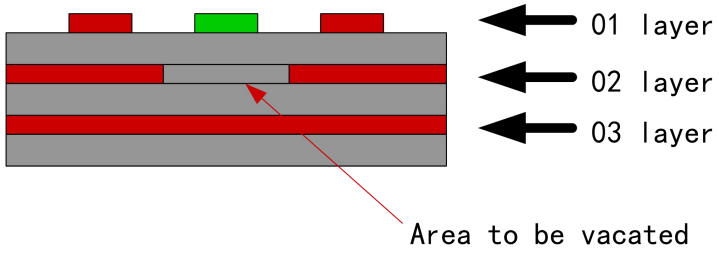


Figure 3-34 Reference ground is the third layer PCB microstrip transmission line structure

3.19.5 RF connector size

✧ If the RF connector is used, the antenna connector must use a coaxial connector with a 50 ohm characteristic impedance.

✧ Hirose's UF.L-R-SMT connector is recommended.

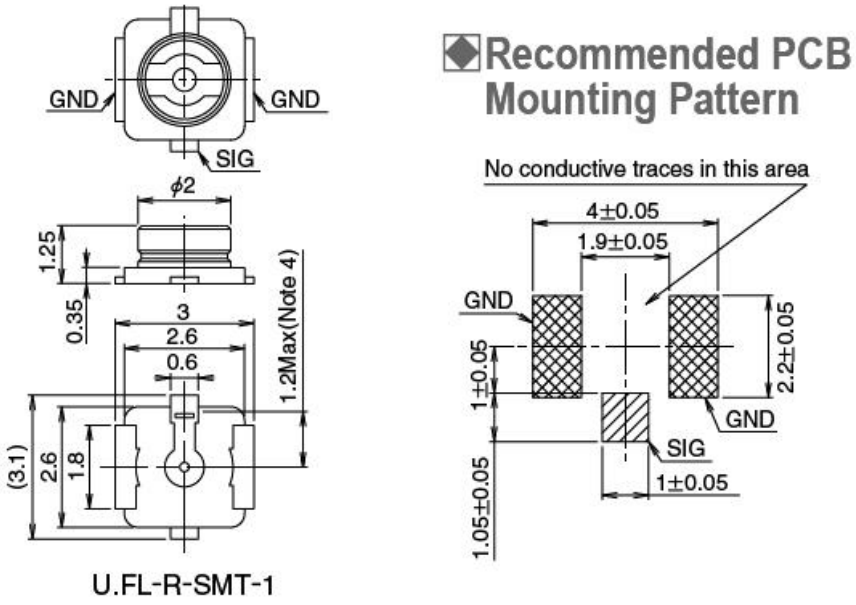


Figure 3-35 RF connector size chart

The RF connector plug for this connector is HRS's U.FL-LP series.

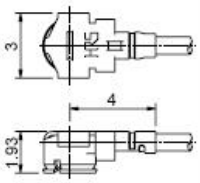
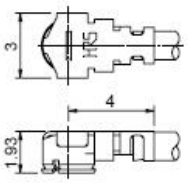
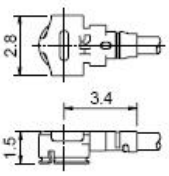
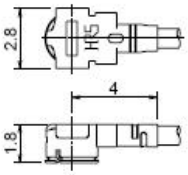
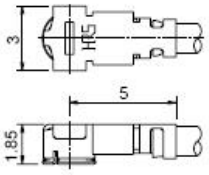
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 3-36 Antenna connector matching plug diagram

Table 3-29 Main parameters of the RF connector

Rated condition		Environmental conditions
Frequency Range	DC to 6GHZ	－40° C to +85° C
Characteristic impedance	50 Ω	－40° C to +85° C

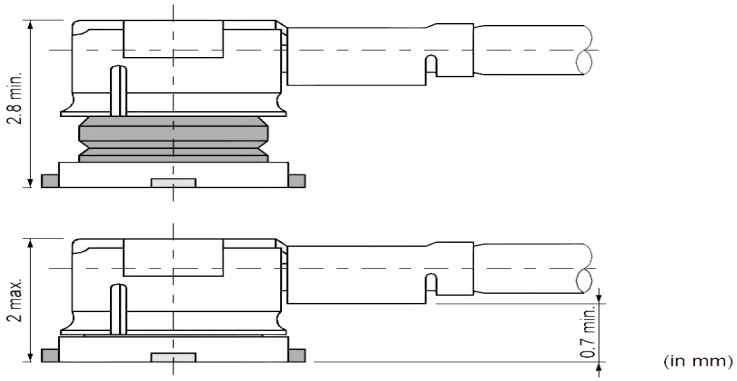


Figure 3-37 Matching coaxial RF line size

Chapter 4 Overall technical indicators

4.1 Chapter overview

- ✧ The CLM920 TD3 module RF overall specifications include the following sections:
- ✧ working frequency
- ✧ Conducted radio frequency measurement
- ✧ Conducted receiving sensitivity and transmit power
- ✧ GNSS reception performance
- ✧ Antenna requirements
- ✧ Module power consumption characteristics

4.2 GNSS reception performance

Table 4-1 Main parameters of GNSS

Parameter	Description	Min	Typical	Max	unit
GPS L1 frequency	Center frequency 1575MHz	1574.4		1576.4	MHz
GLONASS frequency	Center frequency 1601.7MHz	1597.5		1605.9	MHz
BeiDou frequency	Center frequency 1561MHz	1559.1		1563.1	MHz
Galileo E1	Center frequency 1575.42MHz	1573.4		1577.5	MHz
GNSS support channel	55 channels				
GNSS positioning accuracy	Unobstructed open space	2.5	3		M
GNSS sensitivity	Cold start		-145		dBm
GNSS sensitivity	Recapture		-157		dBm
GNSS sensitivity	track		-158		dBm
GNSS positioning time	Cold start		35		S
GNSS positioning time	Warm start		30		S
GNSS positioning time	Hot Start		2		S
GNSS update frequency	Default 1Hz		1		Hz
GNSS data format	NMEA-0183				

GNSS current consumption			80	100	mA

4.3 Working frequency

Table 4-2 RF frequency table

Frequency band	Uplink frequency	Download frequency	Duplex mode
LTE B1	1920MHz - 1980MHz	2110MHz - 2170MHz	FDD
LTE B2	1850MHz - 1910MHz	1930MHz - 1990MHz	FDD
LTE B3	1710MHz - 1785MHz	1805MHz - 1880MHz	FDD
LTE B4	1710MHz - 1755MHz	2110MHz - 2155MHz	FDD
LTE B5	824MHz - 849MHz	869MHz - 894MHz	FDD
LTE B7	2500MHz - 2570MHz	2620MHz - 2690MHz	FDD
LTE B8	880MHz - 915MHz	925MHz - 960MHz	FDD
LTE B12	699MHz - 716MHz	729MHz - 746MHz	FDD
LTE B13	777MHz - 787MHz	746MHz - 756MHz	FDD
LTE B17	704MHz - 716MHz	734MHz - 746MHz	FDD
LTE B25	1850MHz - 1915MHz	1930MHz - 1995MHz	FDD
LTE B26	814MHz - 849MHz	859MHz - 894MHz	FDD
LTE B28	703MHz - 748MHz	758MHz - 803MHz	FDD
LTE B66	1710MHz - 1780MHz	2110MHz - 2180MHz	FDD
LTE B40	2300MHz - 2400MHz	2300MHz - 2400MHz	TDD
LTE B41	2555MHz - 2655MHz	2555MHz - 2655MHz	TDD
GSM850	824MHz - 849MHz	869MHz - 894MHz	GSM
GSM900	880MHz - 915MHz	925MHz - 960MHz	GSM
GSM1800	1710MHz - 1785MHz	1805MHz - 1880MHz	GSM
UMTS B1	1920MHz - 1980MHz	2110MHz - 2170MHz	WCDMA
UMTS B2	1850MHz - 1910MHz	1930MHz - 1990MHz	WCDMA
UMTS B4	1710MHz - 1755MHz	2110MHz - 2155MHz	WCDMA
UMTS B5	824MHz - 849MHz	869MHz - 894MHz	WCDMA
UMTS B8	880MHz - 915MHz	925MHz - 960MHz	WCDMA

4.4 Conducted radio frequency measurement

4.4.1 Test environment

Table 4-3 Test instruments

Test instrument	Power supply	Murata coaxial RF line
R&S CMW500	Agilent 66319	MXHP32HP1000

4.4.2 Test Standard

The CLM920 TD3 module passes the 3GPP TS 51.010-1, 3GPP TS 34.121-1, 3GPP TS 36.521-1, 3GPP2 C.S0011 and 3GPP2 C.S0033 test standards. Each module passes rigorous testing at the factory to ensure reliable quality.

4.5 Conducted receiving sensitivity and transmit power

CLM920 TD3 module 2G and 3G receiving sensitivity and transmit power test indicators are as follows：

Table 4-4 2G3G RF indicators

Mode	Uplink	Download	Power	Receiving sensitivity
GSM 850	824MHz–849MHz	869MHz–894MHz	33±2dBm	<-108dBm
GSM 900	880MHz–915MHz	925MHz–960MHz	33±2dBm	<-109dBm
GSM 1800	1710MHz–1785MHz	1805MHz–1880MHz	30±2dBm	<-109dBm
WCDMA B1	1920MHz–1980MHz	2110MHz–2170MHz	23+2/-2dBm	<-109dBm
WCDMA B2	1850MHz–1910MHz	1930MHz–1990MHz	23+2/-2dBm	<-109dBm
WCDMA B4	1710MHz–1755MHz	2110MHz–2155MHz	23+2/-2dBm	<-109dBm
WCDMA B5	824MHz–849MHz	869MHz–894MH	23+2/-2dBm	<-109dBm
WCDMA B8	880MHz–915MHz	925MHz–960MHz	23+2/-2dBm	<-109dBm

CLM920 TD3 module 4G receiving sensitivity and transmit power test indicators are as follows：

Table 4-5 4G RF sensitivity indicators

Directory (sensitivity)	Directory (sensitivity)	Min	Typical	Max

LTE B1(FDD QPSK pass>95%)	< - 97(10MHz)		-100	-99
LTE B2(FDD QPSK pass>95%)	< - 95(10MHz)		-99	-98
LTE B3(FDD QPSK pass>95%)	< - 94(10MHz)		-98	-97
LTE B4(FDD QPSK pass>95%)	< - 97(10MHz)		-100	-99
LTE B5(FDD QPSK pass>95%)	< - 95(10MHz)		-99	-98
LTE B7(FDD QPSK pass>95%)	< - 95(10MHz)		-98	-97
LTE B8(FDD QPSK pass>95%)	< - 94(10MHz)		-98	-97
LTE B12(FDD QPSK pass>95%)	< - 94(10MHz)		-98	-97
LTE B13(FDD QPSK pass>95%)	< - 94(10MHz)		-98	-97
LTE B17(FDD QPSK pass>95%)	< - 94(10MHz)		-98	-97
LTE B25(FDD QPSK pass>95%)	< - 93.5(10MHz)		-97	-96
LTE B26(FDD QPSK pass>95%)	< - 94.5(10MHz)		-98	-97
LTE B28(FDD QPSK pass>95%)	< - 95.5(10MHz)		-99	-98
LTE B66(FDD QPSK pass>95%)	< - 96.5(10MHz)		-96	-95
LTE B40(TDD QPSK pass>95%)	< - 97(10MHz)		-100	-99
LTE B41(TDD QPSK pass>95%)	< - 95(10MHz)		-98	-97

Table 4-6 4G RF transmit power indicators

Directory (sensitivity)	Directory (sensitivity)	Min	Typical	Max
LTE B1	21 to 25	22	23	24
LTE B2	21 to 25	22	23	24
LTE B3	21 to 25	22	23	24
LTE B4	21 to 25	22	23	24
LTE B5	21 to 25	22	23	24
LTE B7	21 to 25	22	23	24
LTE B8	21 to 25	22	23	24
LTE B12	21 to 25	22	23	24
LTE B13	21 to 25	22	23	24
LTE B17	21 to 25	22	23	24
LTE B25	21 to 25	22	23	24
LTE B26	21 to 25	22	23	24
LTE B28	21 to 25	22	23	24

LTE B66	21 to 25	22	23	24
LTE B40	21 to 25	22	23	24
LTE B41	21 to 25	22	23	24

4.6 Antenna requirements

CLM920 TD3 module main set antenna and GNSS antenna design requirements:

Table 4-7 Main set antenna indicator requirements

Frequency band	Standing wave ratio	Active antenna gain	effectiveness	TRP	TIS
GSM900	<2.5:1	〉-4dbi	〉40%	29	<-102
GSM1800	<2.5:1	〉-4dbi	〉40%	26	<-102
B1 FDD	<2.5:1	〉-4dbi	〉40%	19	<-94
B2 FDD	<2.5:1	〉-4dbi	〉40%	19	<-92
B3 FDD	<2.5:1	〉-4dbi	〉40%	19	<-91
B4 FDD	<2.5:1	〉-4dbi	〉40%	19	<-94
B5 FDD	<2.5:1	〉-4dbi	〉40%	19	<-94
B7 FDD	<2.5:1	〉-4dbi	〉40%	19	<-92
B8 FDD	<2.5:1	〉-4dbi	〉40%	19	<-94
B12 FDD	<2.5:1	〉-4dbi	〉40%	19	<-93
B13 FDD	<2.5:1	〉-4dbi	〉40%	19	<-93
B17 FDD	<2.5:1	〉-4dbi	〉40%	19	<-93
B25 FDD	<2.5:1	〉-4dbi	〉40%	19	<-91
B26 FDD	<2.5:1	〉-4dbi	〉40%	19	<-92
B28 FDD	<2.5:1	〉-4dbi	〉40%	19	<-93
B66 FDD	<2.5:1	〉-4dbi	〉40%	19	<-94
B40 TDD	<2.5:1	〉-4dbi	〉40%	19	<-93
B41 TDD	<2.5:1	〉-4dbi	〉40%	19	<-93
WCDMA B1	<2.5:1	〉-4dbi	〉40%	19	<-106
WCDMA B2	<2.5:1	〉-4dbi	〉40%	19	<-106
WCDMA B4	<2.5:1	〉-4dbi	〉40%	19	<-106
WCDMA B5	<2.5:1	〉-4dbi	〉40%	19	<-106
WCDMA B8	<2.5:1	〉-4dbi	〉40%	19	<-106

Table 4-8 GNSS antenna specifications

Frequency band	Standing wave ratio	Active antenna noise figure	Active antenna gain	Active antenna embedded LNA gain
GPS L1 1575.41+/1.023MHZ	<2:1	<1.5DB	>-2DBi	20DB
GLONASS 1597.5-1605.8MHZ	<2:1	<1.5DB	>-2DBi	20DB
BeiDou 1559.05-1563.14MHZ	<2:1	<1.5DB	>-2DBi	20DB
Galileo E1 1573.4-1577.5MHZ	<2:1	<1.5DB	>-2DBi	20DB

4.7 Power consumption characteristics

Table 4-9 Sleep and idle power consumption of the three major operators (GNSS off)

Operator	System	condition	mode	Current consumption mA
CMCC	GSM	GPS off, no USB connection	Sleep mode	1.5
			Idle mode	18.1
	LTE	GPS off, no USB connection	Sleep mode	1.0
			Idle mode	12.6
CUCC	GSM	GPS off, no USB connection	Sleep mode	2.3
			Idle mode	17.9
	WCDMA	GPS off, no USB connection	Sleep mode	2.3
			Idle mode	17.9
	LTE	GPS off, no USB connection	Sleep mode	2.3
			Idle mode	17.9
CTCC	LTE	GPS off, no USB connection	Sleep mode	1.6
			Idle mode	17.2
	SRLTE	GPS off, no USB connection	Sleep mode	2.2
			Idle mode	18.0

Table 4-10 Call Power Consumption (GNSS Off)

Frequency band	Power level	Current consumption mA
EGSM900	5	270
DCS1800	0	190
WCDMA B1	24dBm	480
WCDMA B2	24dBm	465
WCDMA B4	24dBm	475
WCDMA B5	24dBm	460
WCDMA B8	24dBm	470

Table 4-11 GPRS data transmission power consumption (GNSS off)

Frequency band	Condition	Power level	Current consumption mA
EGSM900	1 receive 4 send	5	280
DCS1800	1 receive 4 send	0	190
EGSM900	1 receive 4 send	5	480
DCS1800	1 receive 4 send	0	460

Table 4-12 EDGE Data Transmission Power Consumption (GNSS Off)

Frequency band	Condition	Power level	Current consumption mA
EGSM900	1 receive 4 send	8	280
DCS1800	1 receive 4 send	2	320
EGSM900	1 receive 4 send	8	220
DCS1800	1 receive 4 send	2	210

Table 4-13 HSDPA data transmission power consumption (GNSS off)

Frequency band	Power dBm	Current consumption mA
WCDMA B1	23	440
WCDMA B2	23	460
WCDMA B4	23	440
WCDMA B5	23	430
WCDMA B8	23	450

Table 4-14 LTE data transmission power consumption (GNSS off)

Frequency band	Test bandwidth	Current consumption mA
LTE-FDD B1	@5Mbps	590
	@10Mbps	610
	@20Mbps	650
LTE-FDD B2	@5Mbps	560
	@10Mbps	580
	@20Mbps	600
LTE-FDD B3	@5Mbps	570
	@10Mbps	590
	@20Mbps	660
LTE-FDD B5	@5Mbps	540
	@10Mbps	560
LTE-FDD B7	@5Mbps	585
	@10Mbps	620
	@20Mbps	680
LTE-FDD B8	@5Mbps	560
	@10Mbps	550
LTE-FDD B12	@5Mbps	545
	@10Mbps	560
LTE-FDD B17	@5Mbps	530
	@10Mbps	550
LTE-FDD B25	@5Mbps	565
	@10Mbps	590
	@20Mbps	640
LTE-FDD B26	@5Mbps	550
	@10Mbps	570
LTE-FDD B28	@5Mbps	550
	@10Mbps	580
	@20Mbps	600
LTE-FDD B66	@5Mbps	580
	@10Mbps	610

	@20Mbps	650
LTE-TDD B40	@5Mbps	330
	@10Mbps	335
	@20Mbps	370
LTE-TDD B41	@5Mbps	320
	@10Mbps	329
	@20Mbps	360

Chapter 5 Interface electrical characteristics

5.1 Chapter overview

- ✧ Working storage temperature
- ✧ Module IO level
- ✧ power supply
- ✧ Electrostatic property
- ✧ Reliability index

5.2 Working storage temperature

Table 5-1 CLM920 TD3 module working storage temperature

parameter	Minimum	Maximum
Normal operating temperature	-35° C	75° C
Extreme working temperature	-40° C	85° C
Storage temperature	-40° C	85° C

5.3 Module IO level

CLM920 TD3 module IO level is as follows：

Table 5-2 Electrical Characteristics of CLM920 TD3 Module

Parameter	Parameter Description	Minimum value	Maximum
VIH	High level input voltage	0.65* VDD_EXT	VDD_EXT+0.3V
VIL	Low level input voltage	-	0.35*VDD_EXT
VOH	High level output voltage	VDD_EXT-0.45V	VDD_EXT
VOL	Low level output voltage	0	0.45V

5.4 Power supply

CLM920 TD3 module input power requirements are as follows：

Table 5-3 Working voltage of CLM920 TD3 module

Parameter	Minimum	Typical	Maximum
Input voltage	3.3V	3.7V	4.2V

The power-on time of any interface of the module must not be earlier than the boot time of the module, otherwise the module may be abnormal or damaged.

5.5 Electrostatic property

There is no overvoltage protection inside the CLM920 TD3 module. The ESD protection is required when the module is used to ensure product quality.

EMC design recommendations:

✧ The USB port needs to add TVS on VDD, D+, D- for protection, and the TVS parasitic capacitance on D+/D- is <2pF;

✧ The module's USIM card external pin needs to be protected by TVS, and the parasitic capacitance requirement is <10pF.

✧ At the module input power supply, increase the TVS. It is recommended that the clamp voltage VCL (Clamping Voltage) is less than 12V and the peak power PPP (Peak Pulse Power) is not less than 100W.

✧ The PCB layout of the protective device should be as close as possible to the "V" line to avoid the "T" line.

✧ The ground plane around the module guarantees integrity and should not be split.

✧ ESD control of the surrounding environment and operators is required during module production, assembly and laboratory testing.

Table 5-4 CLM920 TD3 ESD Features

Test port	Contact discharge	Air discharge	unit
USB interface	±4	±8	KV
USIM interface	±4	±8	KV
Analog voice interface	±4	±8	KV
VBAT power supply	±4	±8	KV

5.6 Reliability index

Table 5-5 CLM920 TD3 reliability test

Test items	Test Conditions	Guideline	Test Results
Low temperature work	Temperature: －40℃ Working mode: normal work Test duration: 24h	IEC60068-2-1	Visual inspection: normal Function check: normal RF indicator check: normal
High	Temperature: 85℃	JESD22-	Visual inspection: normal

temperatur e work	Working mode: normal work Test duration: 24h	A108-C	Function check: normal RF indicator check: normal
Temperatur e cycle	High temperature: 85℃ Low temperature: －40℃ Working mode: normal work Test duration: 30 Cycles;1h+1h/cycle	JESD22-A105-B	Visual inspection: normal Function check: normal RF indicator check: normal
Alternating hot and humid	High temperature: 55 ° C Low temperature: 25 ° C Humidity: 95% ± 3% Working mode: normal work Test duration: 6 Cycles;12h+12h/cycle	JESD22-A101-B	Visual inspection: normal Function check: normal RF indicator check: normal
Temperatur e shock	High temperature: 85 ° C Low temperature: －40 ° C Temperature change time: <30s Working mode: no packaging, no Power on, do not boot Test duration: 100 Cycles;15min+15min/cycle	JESD22-A106-B	Visual inspection: normal Function check: normal RF indicator check: normal
Drop test	Height 0.8m, 6 sides each time, dropped to the horizontal marble platform Working mode: no packaging, no Power on, do not boot	IEC60068-2-32	Visual inspection: normal Function check: normal RF indicator check: normal
Low temperatur e storage	Temperature: －40 ° C Working mode: no packaging, no power, no boot Test duration: 24 h	JESD22-A119-C	Visual inspection: normal Function check: normal RF indicator check: normal
High temperatur e storage	Temperature: 85 ° C Working mode: no packaging, no power, no boot Test duration: 24h	JESD22-A103-C	Visual inspection: normal Function check: normal RF indicator check: normal

Chapter 6 Structural and mechanical properties

6.1 Chapter overview

- ✧ Exterior
- ✧ Module mechanical size

6.2 Exterior

The CLM920 TD3 module is a PCBA with a single-sided layout. The appearance of the module is as follows：

Figure 6-1 Appearance of the CLM920 TD3

6.3 CLM920 TD3 Module mechanical size

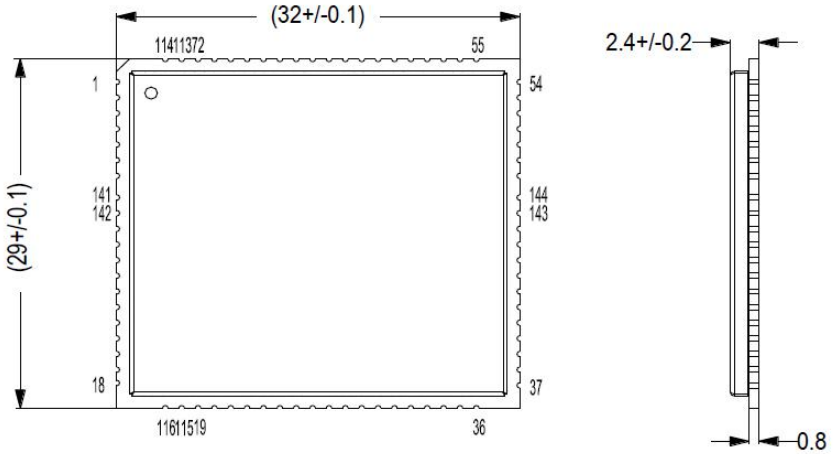


Figure 6-2 Front view and side view of the module (unit: mm)

The figure below shows the bottom view size of the module：

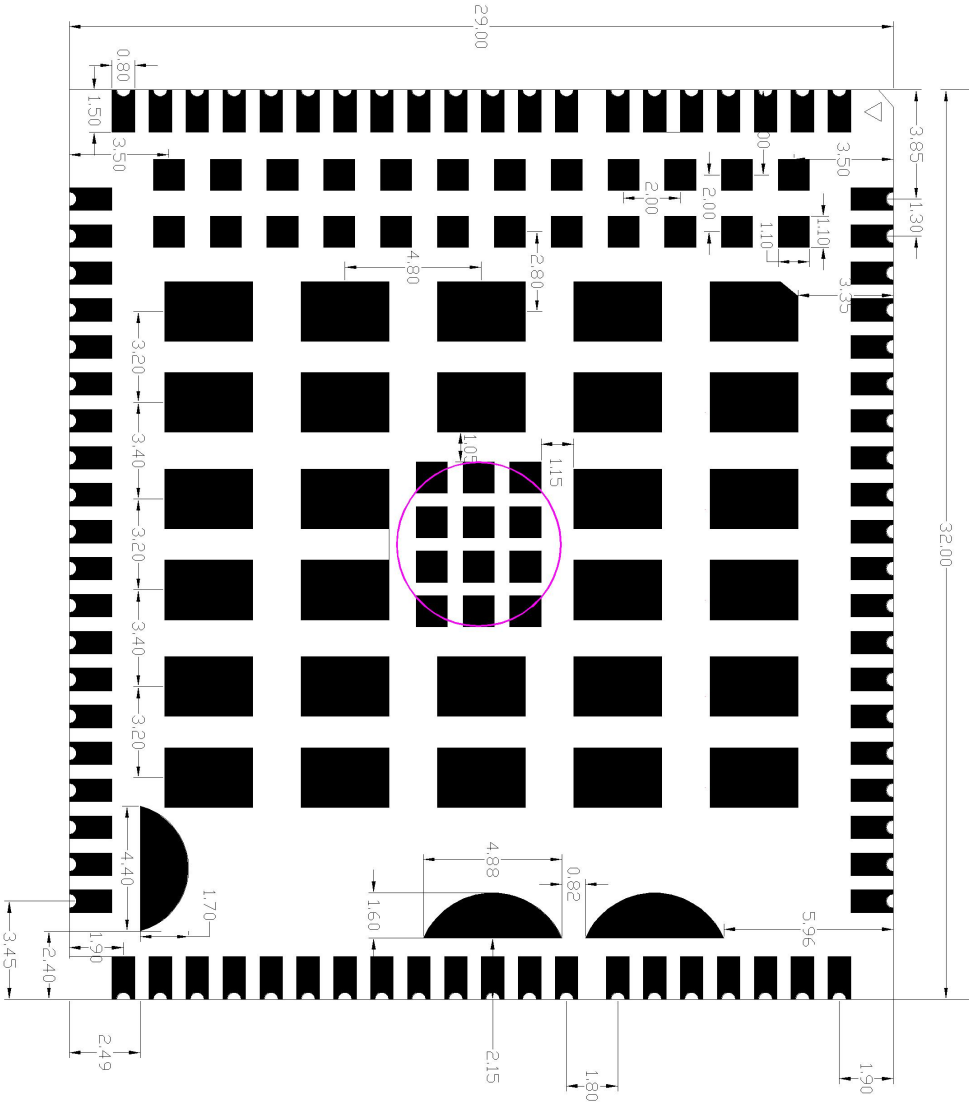


Figure 6-3 Bottom view of the module (unit: mm)

Module recommended package：

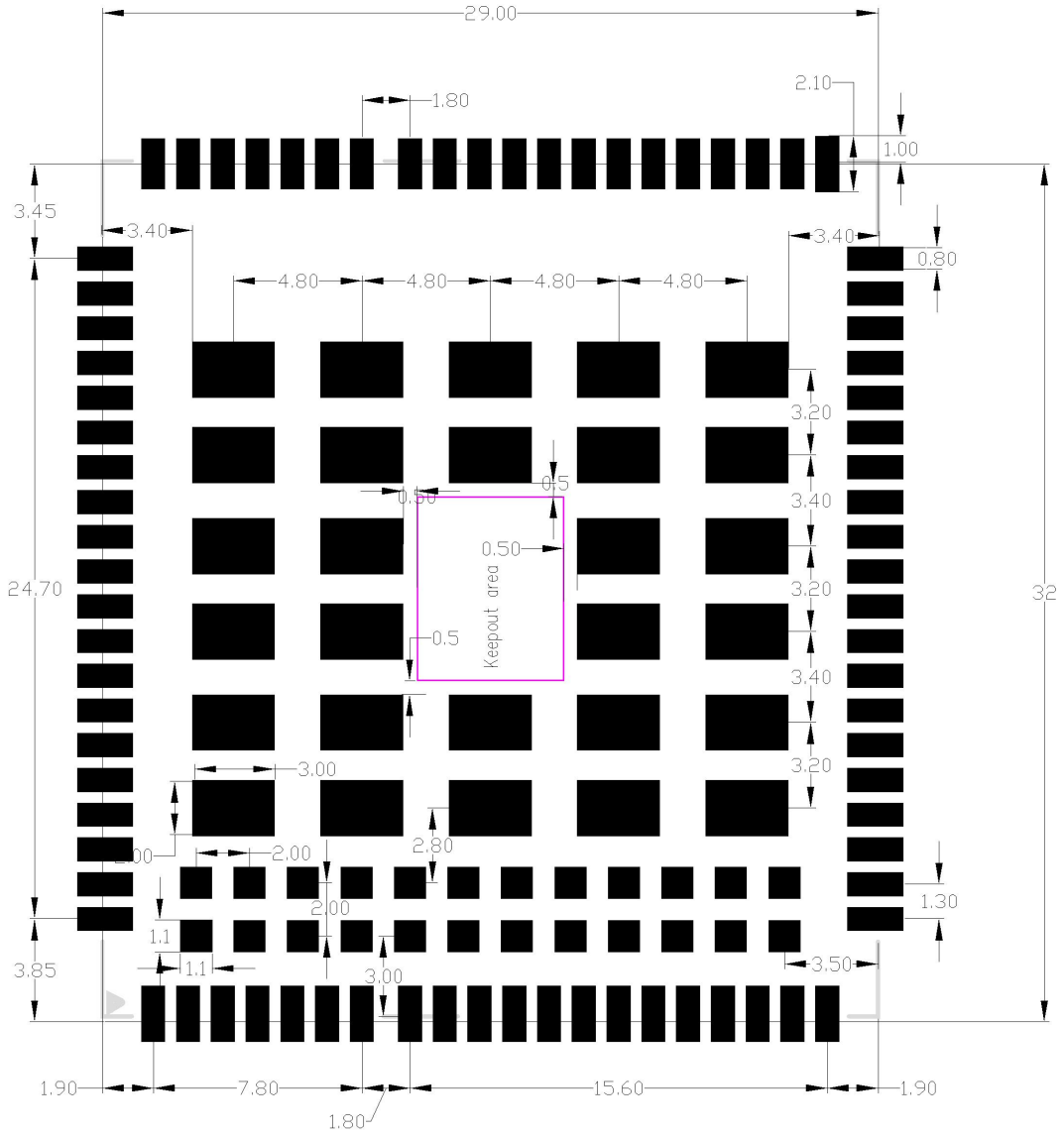


Figure 6-4 Recommended module package (unit: mm)

Chapter 7 Packaging and production

7.1 Chapter overview

- ✧ Module packaging and storage
- ✧ Production welding

7.2 Module packaging and storage

The CLM920 TD3 module is packaged in a tray and packaged in a vacuum sealed bag, with a 10PCS package and a 100PCS package, shipped as a vacuum sealed bag.

The storage of the CLM920 TD3 module module is subject to the following conditions:

- ✧ The module has a moisture sensitivity rating of 3.
- ✧ When the ambient temperature is greater than 40 degrees Celsius and the air humidity is less than 90%, the module can be stored in a vacuum sealed bag for 12 months.
- ✧ When the vacuum sealed bag is opened, if the ambient temperature of the module is lower than 30 degrees Celsius and the air humidity is less than 60%, the factory can complete the patch within 72 hours, and the module can directly perform reflow soldering or other high temperature process.
- ✧ If the module is in other conditions, it needs to be baked before the patch.
- ✧ If the module needs to be baked, please remove the module and bake it for 8 hours at 125 degrees Celsius (allowing fluctuations of up to 5 degrees Celsius).

7.3 Production welding

The CLM920 TD3 module is packaged in an anti-static tray. The SMT line body needs to be equipped with a Tray module. It is recommended to use a reflow oven above 7 temperature zones.

- ✧ To ensure the quality of the module paste, the thickness of the stencil corresponding to the pad portion of the CLM920 TD3 module is recommended to be 0.18 mm.
- ✧ The recommended reflow temperature is 235~245oC, which cannot exceed 260oC.
- ✧ When the PCB is laid out on both sides, the LGA module layout must be machined on the second side. Avoid module falling parts, welding and welding, and poor internal welding of the module caused by the gravity of the module.

The recommended furnace temperature curve is shown below：

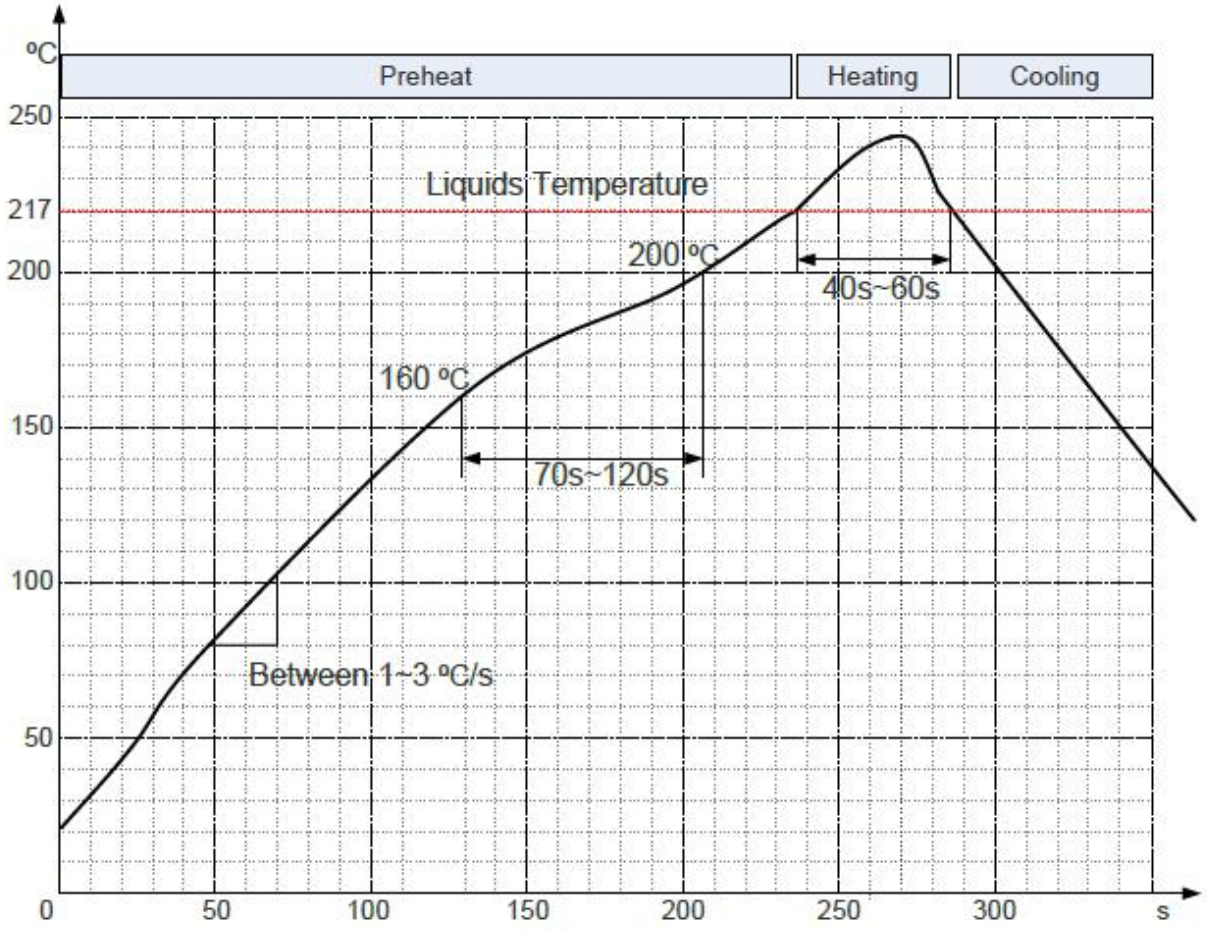


Figure 7-1 Reflow soldering temperature graph

Table 7-1 Reflow process parameter table

Warm zone	Time	Key parameter
Preheating zone (40℃ ~ 165℃)		Heating rate: 1℃ / s ~ 3℃ / s
Temperature zone (160℃ ~210℃)	(t1～t2)：70s～120s	
Recirculation zone (>217℃)	(t3～t4)：40s～60s	Peak temperature: 235℃ ~ 245℃
Cooling zone	Cooling rate: 2℃ / s ≤ Slope ≤ 5℃ / s	

Chapter8 Appendix

8.1 Chapter overview

- ✧ Abbreviations
- ✧ Encoding
- ✧ Safety and precautions

8.2 Abbreviations

Table 8-1 Abbreviations

Abbreviations	Full name
3GPP	Third Generation Partnership Project
AP	Access Point
AMR	Adaptive Multi-rate
BER	Bit Error Rate
CCC	China Compulsory Certification
CDMA	Code Division Multiple Access
CE	European Conformity
CSD	Circuit Switched Data
CTS	Clear to Send
DC	Direct Current
DTR	Data Terminal Ready
DL	Down Link
DTE	Data Terminal Equipment
DRX	Discontinuous Reception
EDGE	Enhanced Data Rate for GSM Evolution
EU	European Union
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FCC	Federal Communications Commission
GPRS	General Packet Radio Service
GSM	Global System for Mobile Communication
HSDPA	High-Speed Downlink Packet Access

HSPA	Enhanced High Speed Packet Access
HSUPA	High Speed Up-link Packet Access
IMEI	International Mobile Equipment Identity
LED	Light-Emitting Diode
LTE	Long Term Evolution
NC	Not Connected
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PMU	Power Management Unit
PPP	Point-to-point protocol
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RoHS	Restriction of the Use of Certain Hazardous Substances
SMS	Short Message Service
TIS	Total Isotropic Sensitivity
TVS	Transient Voltage Suppressor
TX	Transmitting Direction
UART	Universal Asynchronous Receiver-Transmitter
UMTS	Universal Mobile Telecommunications System
USIM	Universal Subscriber Identity Module
USSD	Unstructured Supplementary Service Data
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WWAN	Wireless Wide Area Network

8.3 Encoding

Table 8-2 Time slot allocation table for different levels of GPRS/EDGE

Slot class	DL slot number	UL slot number	Active slot number
1	1	1	2
2	2	1	3

3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5

Table 8-3 Maximum GPRS rate

GPRS coding scheme	Max data rata(4 slots)	Modulation type
CS 1=9.05kb/s/time slot	36.2kb/s	GMSK
CS 2=13.4kb/s/time slot	53.6kb/s	GMSK
CS 3=15.6kb/s/time slot	62.4kb/s	GMSK
CS 4=21.4kb/s/time slot	85.6kb/s	GMSK

Table 8-4 Maximum EDGE Rate

GPRS coding scheme	Max data rata(4 slots)	Modulation type
MCS 1=8.8kb/s/time slot	35.2kb/s	GMSK
MCS 2=11.2kb/s/time slot	44.8kb/s	GMSK
MCS 3=14.8kb/s/time slot	59.2kb/s	GMSK
MCS 4=17.6kb/s/time slot	70.4kb/s	GMSK
MCS 5=22.4kb/s/time slot	89.6kb/s	8PSK
MCS 6=29.6kb/s/time slot	118.4kb/s	8PSK
MCS 7=44.8kb/s/time slot	179.2kb/s	8PSK
MCS 8=54.4kb/s/time slot	217.6kb/s	8PSK
MCS 9=59.2kb/s/time slot	236.8kb/s	8PSK

Table 8-5 Maximum HSDPA rate

HSDPA device category	Max data rate(peak)	Modulation type

Category 1	1.2Mbps	16QAM,QPSK
Category 2	1.2Mbps	16QAM,QPSK
Category 3	1.8Mbps	16QAM,QPSK
Category 4	1.8Mbps	16QAM,QPSK
Category 5	3.6Mbps	16QAM,QPSK
Category 6	3.6Mbps	16QAM,QPSK
Category 7	7.2Mbps	16QAM,QPSK
Category 8	7.2Mbps	16QAM,QPSK
Category 9	10.2Mbps	16QAM,QPSK
Category 10	14.4Mbps	16QAM,QPSK
Category 11	0.9Mbps	QPSK
Category 12	1.8Mbps	QPSK
Category 13	17.6Mbps	64QAM
Category 14	21.1Mbps	64QAM
Category 15	23.4Mbps	16QAM
Category 16	28Mbps	16QAM
Category 17	23.4Mbps	64QAM
Category 18	28Mbps	64QAM
Category 19	35.5Mbps	64QAM
Category 20	42Mbps	64QAM
Category 21	23.4Mbps	16QAM
Category 22	28Mbps	16QAM
Category 23	35.5Mbps	64QAM
Category 24	42.2Mbps	64QAM

Table 8-6 Maximum HSUPA rate

HSUPA device category	Max data rate(peak)	Modulation type
Category 1	0.96Mbps	QPSK
Category 2	1.92Mbps	QPSK
Category 3	1.92Mbps	QPSK
Category 4	3.84Mbps	QPSK
Category 5	3.84Mbps	QPSK

Category 6	5.76Mbps	QPSK

Table 8-7 LTE-FDD DL maximum rate

LTE-FDD device category	Max data rate(peak)	Modulation type
Category 1	10Mbps	QPSK/16QAM/64QAM
Category 2	50Mbps	QPSK/16QAM/64QAM
Category 3	100Mbps	QPSK/16QAM/64QAM
Category 4	150Mbps	QPSK/16QAM/64QAM

Table 8-8 LTE-FDD UL Maximum Rate

LTE-FDD device category	Max data rate(peak)	Modulation type
Category 1	5Mbps	QPSK/16QAM
Category 2	25Mbps	QPSK/16QAM
Category 3	50Mbps	QPSK/16QAM
Category 4	50Mbps	QPSK/16QAM

8.4 Safety and precautions

In order to use the wireless device safely, the terminal device is informed of the relevant security information:

✧ Interference: When the use of wireless devices is prohibited or the use of the device causes interference and security of the electronic device, turn off the wireless device. Because the terminal will send and receive RF signals when it is powered on. It can interfere with TV, radio, computer or other electrical equipment.

✧ Medical equipment: In medical and health care facilities where the use of wireless devices is prohibited by express text, please follow the regulations of the site and turn off the device. Some wireless devices may interfere with the medical device, causing the medical device to malfunction or cause errors. If interference occurs, turn off the wireless device and consult a physician.

✧ Flammable and explosive areas: In flammable and explosive areas, please turn off your wireless device and follow the relevant label instructions to avoid an explosion or fire. Such as: gas stations, fuel zones, chemical products areas and chemical transportation and

storage facilities, areas with explosion hazard signs, areas with "turn off radio equipment" signs.

✧ Traffic Safety: Please comply with local laws or regulations in your country or region regarding the use of wireless devices when driving a vehicle.

✧ Aviation Safety: When flying, please follow the airline's regulations and regulations regarding the use of wireless equipment. Before taking off, turn off the wireless device to prevent wireless signals from interfering with aircraft control signals.

✧ Environmental Protection: Please comply with local laws regarding the handling of equipment packaging materials, equipment or accessories, and support recycling operations.

✧ Emergency call: This device uses wireless signals for propagation. Therefore, the network cannot be connected in all cases, so in the emergency, the wireless device cannot be used as the only contact method.