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CLM920_NC5
LTE Module Hardware User Guide

V1.6

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Update records

version	Date	Author	Description
V1.0	20160808	David	Initial
V1.1	20161101	David	1.Modify the analog voice circuit description
V1.2	20161130	David	1. Increase the power supply description 2. Add PCM description
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V1.4	20170323	David	1. Increase WCDMA B5 RF indicator
V1.5	20170421	David	1. Modify the working range of the module through the high and low temperature limit test
V1.6	20170628	David	

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Chart catalog

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Chapter 1. Introduction

This document is a wireless solution product CLM920_NC5 Mini PCIE module hardware interface manual, designed to describe the hardware components and functional characteristics of the module solution product, application interface definition and usage instructions, electrical and mechanical characteristics, etc., for user-based application development of the product Provide hardware instructions.

Abbreviation:

ADC	Analog-Digital Converter
AFC	Automatic Frequency Control
AGC	Automatic Gain Control
ARFCN	Absolute Radio Frequency Channel Number
B2B	Board to Board Connector
BER	Bit Error Rate
CDMA	Code Division Multiple Access
DAI	Digital Audio interface
DAC	Digital-to-Analog Converter
DSP	Digital Signal Processor
DTR	Data Terminal Ready
EFR	Enhanced Full Rate
EMC	Electromagnetic Compatibility
EMI	Electro Magnetic Interference
ESD	Electronic Static Discharge
EVDO	Evolution Data Only
FR	Full Rate
GPRS	General Packet Radio Service
HR	Half Rate
IMEI	International Mobile Equipment Identity
ISO	International Standards Organization
PLL	Phase Locked Loop
PPP	Point-to-point protocol
RAM	Random Access Memory
ROM	Read-only Memory
RTC	Real Time Clock
SMS	Short Message Service
UART	Universal asynchronous receiver-transmitter
UIM	User Identifier Management
USB	Universal Serial Bus
VSWR	Voltage Standing Wave Ratio

Chapter 2. Module review

2.1 Product Introduction

CLM920_NC5 Mini PCIE module is a PCI Express Mini Card 1.2 standard module, which is an integrated FDD-LTE/TDD-LTE/TD-SCDMA/WCDMA/EVDO/CDMA/EDGE
/GSM network standard and GPS positioning service. Wireless terminal products. The module baseband chip adopts Qualcomm's MDM9X07, supports the three major network standards of China Mobile Unicom Telecom, and supports OS: Windows 7/Windows 8/Windows 10/Android 4.0 and above. The CLM920_NC5 module can be used in the following situations:

- ✧ Car Equipment
- ✧ Wireless POS machine
- ✧ Wireless advertising, media
- ✧ Remote monitoring
- ✧ Smart meter reading
- ✧ Mobile broadband
- ✧ automated industry
- ✧ Other wireless terminals, etc.

2.2 Module characteristics

Table 2-1 Module Specifications

Product name	Description
CLM920_NC5	LTE for CMCC,CUCC and CTCC, support SRLTE,GPS and Analog audio
CLM920_TB5	LTE for CMCC,CUCC and CTCC, support GPS， Analog audio， LTE Cat.1 spec （optional）
CLM920_TE5	LTE for CMCC,CUCC and EU, support GPS and Analog audio

Table 2-2 List of module frequency bands

Network Type	Frequency band	Module series		
		CLM920_NC5	CLM920_TB5	CLM920_TE5
GSM	GSM850	√	√	√
	GSM900	√	√	√
	GSM1800	√	√	√
LTE(FDD)	LTE FDD B1	√	√	√
	LTE FDD B3	√	√	√
	LTE FDD B5	√	√	√
	LTE FDD B7			√
	LTE FDD B8	√	√	√
	LTE FDD B20			√
LTE(TDD)	LTE TDD B38	√	√	√
	LTE TDD B39	√	√	√
	LTE TDD B40	√	√	√
	LTE TDD B41	√	√	√
TD-SCDMA	TD-SCDMA B34	√	√	√
	TD-SCDMA B39	√	√	√
WCDMA	BAND 1	√	√	√
	BAND 5	√	√	√
	BAND 8	√	√	√
CDMA2000/EVDO	BC0	√		
GNSS	GLONASS	√	√	√
	GPS	√	√	√
	BeiDou/Compass	√	√	√

NOTE

- ✧ The module chip supports Category 4 by default.
- ✧ The GNSS feature is optional.
- ✧ The diversity function is optional.
- ✧ The CLM920 TB5 supports CAT1 standard modules for customer-specific applications. The CAT1

system has an uplink of 5 Mbps and a downlink of 10 Mbps.

If you have a frequency band or technical requirements, you can contact local technical support for assistance.

Table 2-3 key characteristics

Characteristic	Description
Physical characteristics	51mmx30mmx2.8mm
Fixed way	Ground screw hole (2)
Application processor	Single core ARM Cortex-A7 processor, clocked at 1.2GHZ, 256kB level 2 cache
Operating Voltage	3.3V - 4.2V Typical Voltage 3.7V
Energy saving current	Standby current < 5mA
Application interface	Standard SIM interface, support 3.0V/1.8V, support hot swap function USB2.0 (High-Speed) Hardware reset interface UART serial interface PCM/analog voice interface Power interface Network status indication interface General purpose GPIO interface
Antenna connector	Main set antenna connector (MM4829-2702RA4) Diversity Antenna Connector (MM4829-2702RA4) GPS antenna connector (MM4829-2702RA4)
Transmit power	LTE: Class 3 (23dBm±2dB) UMTS: Class 3 (24dBm+1/-3dB) TD-SCDMA: Class 2 (24dBm+1/-3dB) CDMA2000： Class 3 (24dBm+3/-1dB) GSM/GPRS: Class 4 (33dBm±2dB) GSM850/GSM900 Class 1 (30dBm±2dB) DCS1800/PCS1900
Data service	GSM/EDGE: GPRS: DL 85.6 kbps/UL 85.6 kbps EDGE: DL 236.8 kbps/UL 236.8 kbps WCDMA: UMTS R99： DL 384 kbps/UL 384 kbps DC-HSPA+: DL 42 Mbps/UL 5.76 Mbps TD-SCDMA: TD-HSDPA/HSUPA: 2.2Mbps（UL）/2.8Mbps（DL） EV-DOr0/DOrA

	CDMA 1xEVDOr0: DL 2.4Mbps/UL 153kbps CDMA 1xEVDOrA: DL 3.1Mbps/UL 1.8Mbps LTE: LTE FDD:DL 150Mbps/UL 50Mbps@20M BW cat4 LTE TDD:DL 130Mbps/UL 35Mbps@20M BW cat4 LTE FDD:DL 10Mbps/UL 5Mbps@20M BW cat1 LTE TDD:DL 10Mbps/UL 5Mbps@20M BW cat1
Satellite positioning	GPS/BEIDOU/GLONASS Protocol：NMEA
Diversity antenna	Support LTE diversity antenna
AT command	Support for standard AT instruction sets (Hayes 3GPP TS 27.007 and 27.005)
SMS business	Support Text and PDU mode Support point-to-point MO and MT SMS storage: USIM card / ME (default)
Virtual network card	Support USB virtual network card
Temperature range	Normal operating temperature －35° C to +75° C Extreme operating temperature －40° C to +85° C Storage temperature -40° C to +85° C
Module function distinction	On the label paper, M stands for the main set, D takes the table diversity, G stands for GPS, and V stands for analog voice.

2.3 Module function

The CLM920_NC5 Mini PCIE module mainly consists of the following circuit units:

- ✧ Baseband processing unit
- ✧ Power management unit
- ✧ Memory unit
- ✧ RF transceiver unit
- ✧ RF front end unit
- ✧ GPS RF receiving unit

The functional block diagram of the CLM920_NC5 Mini PCIE module is as follows:

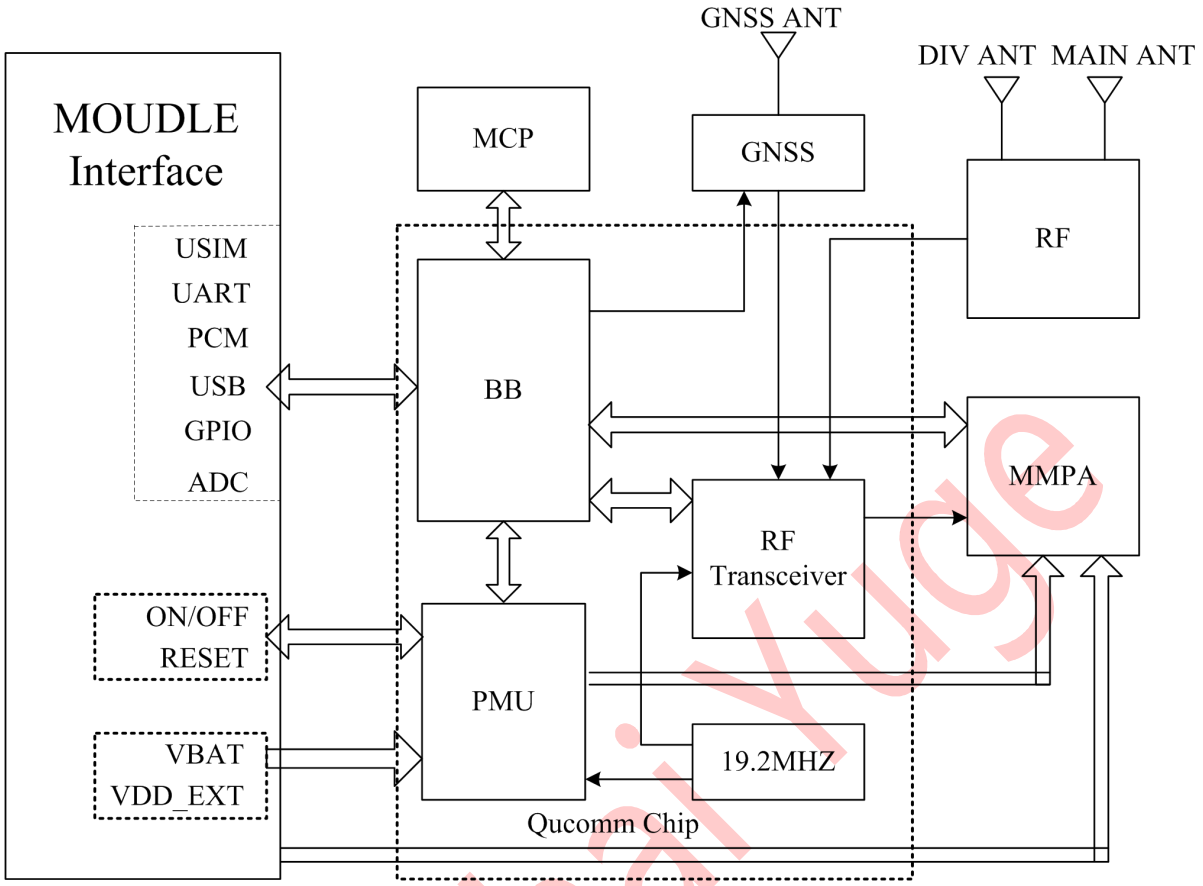


Figure 2-1 Functional block diagram of the CLM920_NC5 Mini PCIE module

Chapter 3. Interface application description

3.1 Overview of this chapter

This chapter mainly describes the interface definition and application of this module. Contains the following sections:

✧ 52-pin gold finger

- ✧ Interface definition
- ✧ Power interface
- ✧ USB interface
- ✧ USIM interface
- ✧ UART interface
- ✧ WWAN control interface
- ✧ PCM/analog voice interface
- ✧ RF antenna interface

3.2 Module interface

3.2.1 52-pin gold finger

The CLM920_NC5 Mini PCIE module uses the 52-pin Mini PCIE Goldfinger as an external interactive interface.

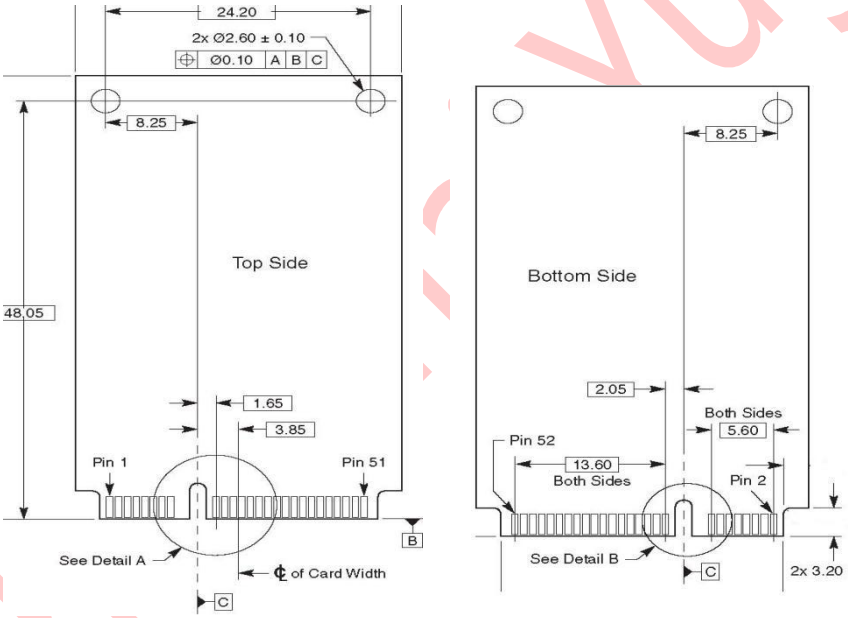
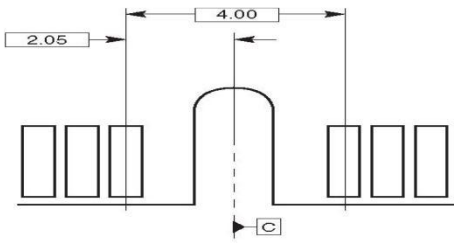


Figure 3-1 Gold finger TOP surface and BOTTOM surface



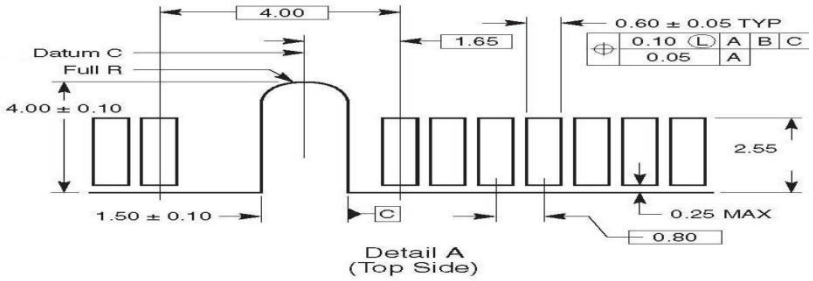


Figure 3-2 Detail of the gold finger TOP and BOTTOM AB

3.2.2 Interface Definition

The CLM920_NC5 Mini PCIE module interface is a standard Mini PCI Express interface. The module interface definitions are shown in the following table:

Table 3-1 IO parameter definition

Symbol sign	Description
IO	Two-way input and output
PI	power input
PO	Power Output
AI	Analog input
AO	Analog output
DI	Digital input
DO	Digital output

Table 3-2 Interface definition

Pin	Standard definition	Module definition	IO	Functional description	Remarks
1	WAKE#	MIC+	AI	Audio input +	
2	3.3Vaux	VBAT	PI	Power input	
3	COEX1	MIC-	AI	Audio input -	
4	GND	GND		Ground	
5	COEX2	SPK+/REC+	AO	Analog output +	AT set headphones and speakers
6	1.5V	UIM_DET	DI	SIM card hot plug detection	
7	CLKREQ#	SPK-/REC-	AO	Analog output -	AT set headphones and speakers
8	UIM_PWR	UIM_PWR	PO	SIM power output	
9	GND	GND		Ground	
10	UIM_DATA	UIM_DATA	IO	SIM data signal	

11	REFCLK-	UART_RX	DI	Serial port receiving signal	
12	UIM_CLK	UIM_CLK	DO	SIM clock signal	
13	REFCLK+	UART_TX	DO	Serial port send signal	
14	UIM_RESET	UIM_RESET	DO	SIM reset signal	
15	GND	GND		Ground	
16	UIM_VPP	NC			
17	RESERVED	VDD_EXT	PO	1.8V output power supply	
18	GND	GND		Ground	
19	RESERVED	WAKEUP_IN	DI	Module sleep control	1.8V, active low
20	W_DISABLE#	W_DISABLE#	DI	Turn off RF communication	Active low
21	GND	GND		Ground	
22	PERST#	RESET	DI	Reset control	Active low
23	PERn0	UART_CTS	DI	Serial port send clear	
24	3.3Vaux	VBAT	PI	Power input	
25	PERp0	UART_RTS	DO	Serial port request to send	
26	GND	GND		Ground	
27	GND	GND		Ground	
28	1.5V	PWRKEY	AI	Power on signal	
29	GND	GND		Ground	
30	SMB_CLK	NC			
31	PETn0	NC			
32	SMB_DATA	WAKEUP_OUT	DO	Module wake up host	
33	PETp0	NC			
34	GND	GND		Ground	
35	GND	GND		Ground	
36	USB_D-	USB_DM	IO	USB differential signal -	
37	GND	GND		Ground	
38	USB_D+	USB_DP	IO	USB differential signal +	
39	3.3Vaux	VBAT	PI	power input	
40	GND	GND		Ground	
41	3.3Vaux	VBAT	PI	power input	
42	LED_WWAN#	LED_WWAN#	OC	Status light indication	
43	GND	GND		Ground	
44	LED_WLAN#	UIM_DET	DI	Hot plug detection	Reserved SIM hot swap
45	RESERVED	PCM_CLK	DO	PCM clock pulse	
46	LED_WPAN#	NC			Reserved status light indication
47	RESERVED	PCM_DOUT	DO	PCM sends data	

48	1.5V	NC			
49	RESERVED	PCM_DIN	DI	PCM receiving data	
50	GND	GND		Ground	
51	RESERVED	PCM_SYNC	DO	Frame synchronization signal	
52	3.3Vaux	VBAT	PI	power input	

NOTE

- ✧ The module typically has an IO port level of 1.8V (in addition to the SIM, the SIM card port level supports 1.8V and 3.0V).
- ✧ This module defines the RESERVED and NC pins to be left unconnected.

3.3 Power Interface

The CLM920_NC5 Mini PCIE module power connector consists of two parts:

- ✧ VBAT is the working power of the module;
- ✧ UIM_PWR is the working power supply for the SIM card;

The power interface of the CLM920_NC5 Mini PCIE module is as follows:

Table 3-3 Power pin definition

Pin number	name	I/O	description	Min	typical	Max
2,24,39,41,52	VBAT	PI	Module power supply	3.3V	3.7V	4.2V
8	UIM_PWR	PO	SIM power supply	0	1.8V/2.85V	1.9/2.95V
17	VDD_EXT	PO	Output power		1.8V	
4,9,15,18,21,26,27,29,34,35,37,40,43,50	GND		Ground	-	0	-

CLM920_NC5 Mini PCIE module adopts single power supply mode, the module provides 5 power supply pins and 14 ground pins. In order to ensure the normal operation of the module, all power and ground pins must be connected. The module power supply range is 3.3-4.2V, and it is recommended to use 3.7V/2A power supply. The module will generate a peak current of more than 2A when transmitting data or talking, resulting in a large ripple on the power supply. Therefore, when designing the circuit, the power supply trace should be kept as short as possible. It is recommended to reserve one 220uF capacitor near the power input. Customers are advised to use DCDC or LDO to provide sufficient current. The VBAT is then powered through the MOS transistor so that the module can be completely powered down. For practical use, please refer to the following circuit design:

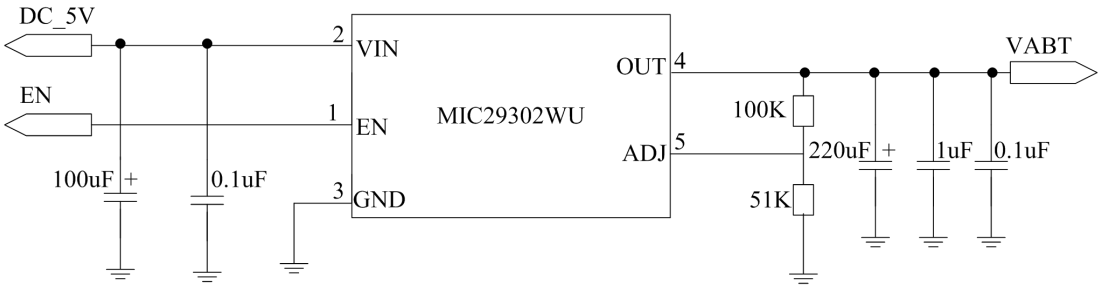


Figure 3-3 LDO power reference circuit

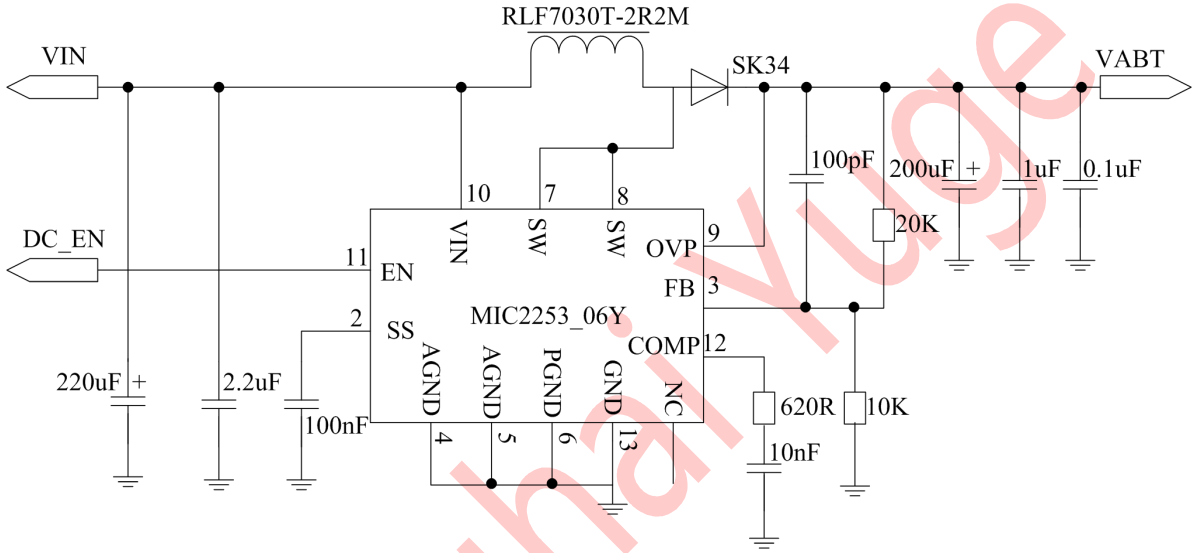


Figure 3-4 DCDC power supply reference circuit

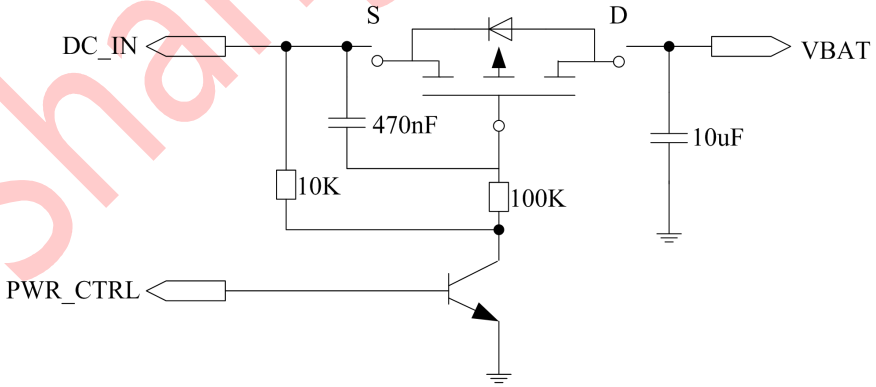


Figure 3-5 MOS tube control power switch reference circuit

NOTE

1. To prevent damage to the module caused by surge and overvoltage, it is recommended to connect a 5.1V/500mW Zener diode in parallel with the VBAT pin of the module.
2. It is recommended to add 3 ceramic capacitors (33pF, 10pF, 100nF) to the VBAT pin and place them near the VBAT pin.
3. The minimum working voltage of the module is 3.3V. Since the transmission data or GSM call will

generate more than 2A current, the ripple voltage drop will occur on the power supply voltage, so the power supply voltage must not be lower than 3.3V.

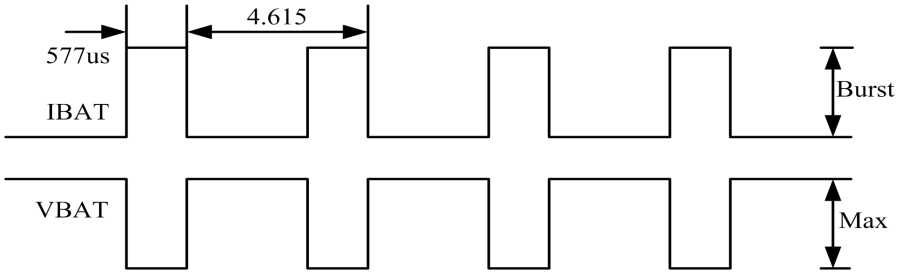


Figure 3-6 GSM TDMA Burst Current Supply Voltage Drop

3.4 Switching machine reset mode

The CLM920_NC5 Mini PCIE module only supports power-on and power-on mode. The user can check whether the module is powered on by querying the high and low levels of the VDD_EXT pin.

Table 3-4 Switching machine reset pin definition

Pin	Signal name	I/O	High value	Description
22	RESET	DI	1.8V	Module reset control pin, low effective
28	PWRKEY	PI	VBAT-0.3V	Low level boot

3.4.1 Boot Timing

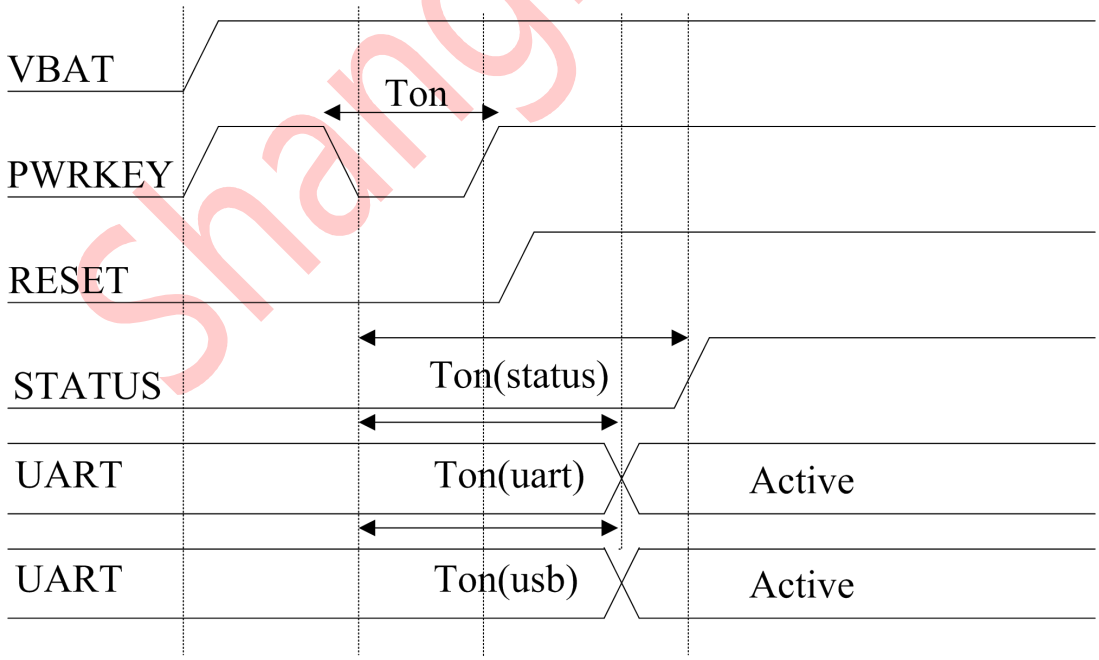


Figure 3-7 Startup timing diagram

Table 3-5 boot timing parameters

Symbol	Description	Min	Typical	Max	Unit
Ton	Boot low level width	100	500	-	mS
Ton(status)	Boot time (according to status status)	22	-	-	S
Ton(usb)	Boot time (according to usb status)	-	20	-	S
Ton(uart)	Boot time (according to uart status)	-	20	-	S
VIH	PWRKEY input high level	0.6	0.8	1.8	V
VIL	PWRKEY input low level	-0.3	0	0.5	V

3.4.2 Power-off shutdown

If the CLM920_NC5 Mini PCIE module is to be shut down, the VBAT power supply can be cut off. At this time, the module does not perform the normal shutdown process. It is recommended that the module be powered off and restarted only when the module fails to restart. It is recommended that the interval between restarts be greater than 30S.

3.4.3 Reset control

CLM920_NC5 Mini PCIE module PIN22 signal is RESET reset pin. When the application needs to reset the module, the module can be reset by pulling the pin low for 150-450ms. The RESET pin is sensitive to interference and is away from RF interference signals when routing.

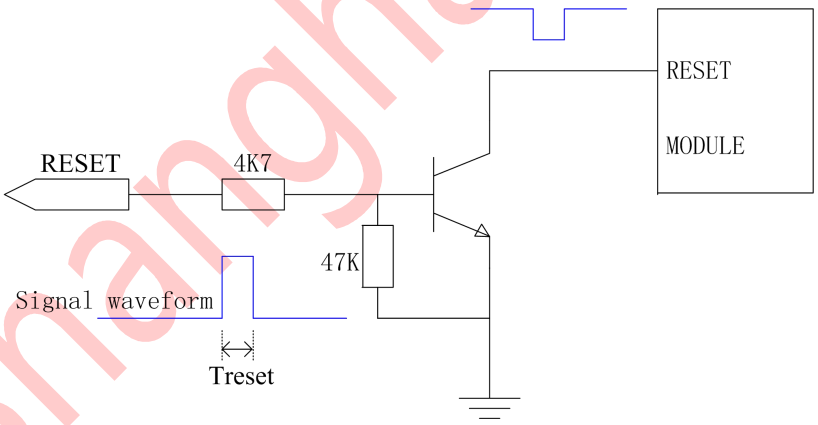


Figure 3-8 Reset Reference Circuit

Table 3-6 RESET pin parameters

Symbol	Description	Min	Typical	Max	Unit
Treset	Low pulse width	150	200	450	ms
VIH	RESET input high level voltage	1.17	1.8	2.1	V
VIL	RESET input low level voltage	-0.3	0	0.8	V

The reset RESET timing is as follows:

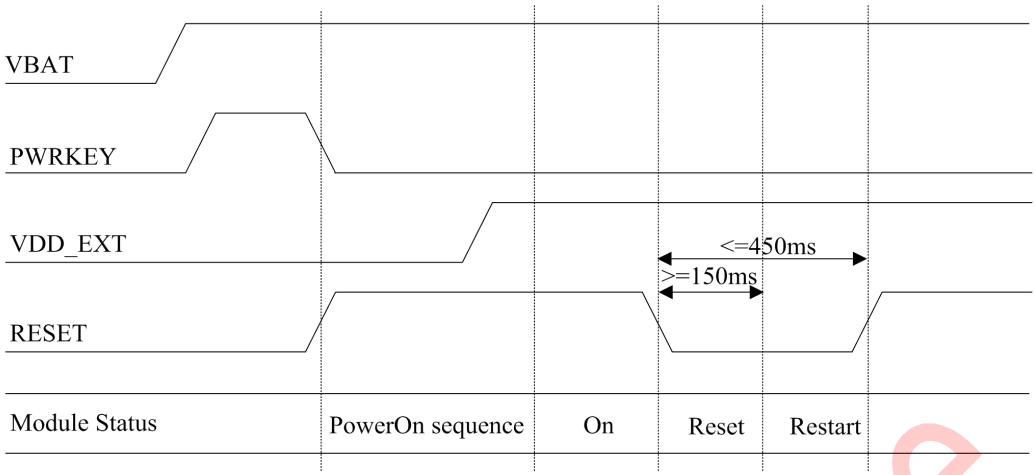


Figure 3-9 Reset timing diagram

The CLM920_NC5 Mini PCIE module supports AT command reset. The AT command is at+cfun=1,1 to restart the module. Detailed instructions can be found in the CLM920_NC5 AT instruction set manual.

3.5 USB interface

CLM920_NC5 Mini PCIE module USB interface supports USB2.0 high-speed protocol, supports slave mode, does not support USB charging mode. USB input and output traces must comply with the USB2.0 feature. The USB interface is defined as follows:

Table 3-7 USB interface pin definition

Pin number	Signal name	IO	Description
36	USB_DM	IO	USB differential signal -
38	USB_DP	IO	USB differential signal +
4,9,15,18,21,26,27,29, 34,35,37,40,43,50	GND		Ground

The module acts as a USB slave device and supports USB sleep and wake-up mechanisms. The reference design circuit is as follows:

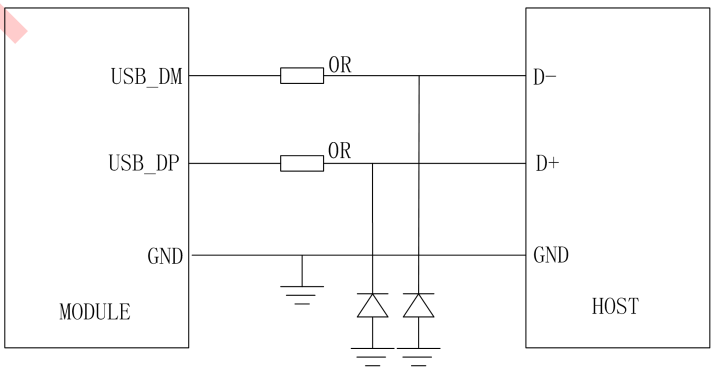


Figure 3-10 USB connection design circuit diagram

NOTE

1.The USB interface supports high-speed (480Mbps) and full-speed (12Mbps) modes. Therefore, the trace design needs to strictly follow the USB2.0 protocol requirements. Pay attention to the protection of the data lines, differential traces, and control impedance of 90Ω.

2.In order to improve the antistatic performance of the USB interface, it is recommended to add an ESD protection device on the data line. The equivalent capacitance of the protection device is less than 2pF.

3.The USB interface bus supply voltage is provided internally by the module and is not required externally. At the same time, since the USB interface of the module does not provide USB bus power, the module can only be used as a slave device of the USB bus device.

The USB interface supports the following features:

- ✧ Software download upgrade
- ✧ Data communication
- ✧ AT Command
- ✧ GNSS NMEA output, etc.

3.6 UART interface

The CLM920_NC5 Mini PCIE module provides a set of UART interfaces with a serial port level of 1.8V. Through the serial port, you can send AT commands, print program log information, and so on.

The module serial port supports 9600, 19200, 38400, 57600, 115200, 230400bps baud rate, the default is 115200bps.

The UART interface is defined as follows:

Table 3-8 UART serial port signal definition

Pin number	Signal name	I/O	Description
11	UART_RX	DI	Serial port receiving data
13	UART_TX	DO	Serial port to send data
23	UART_CTS	DI	User allows module to send
25	UART_RTS	DO	The module requests the user to send

If you need to use the serial port, you need to refer to the following serial port design.

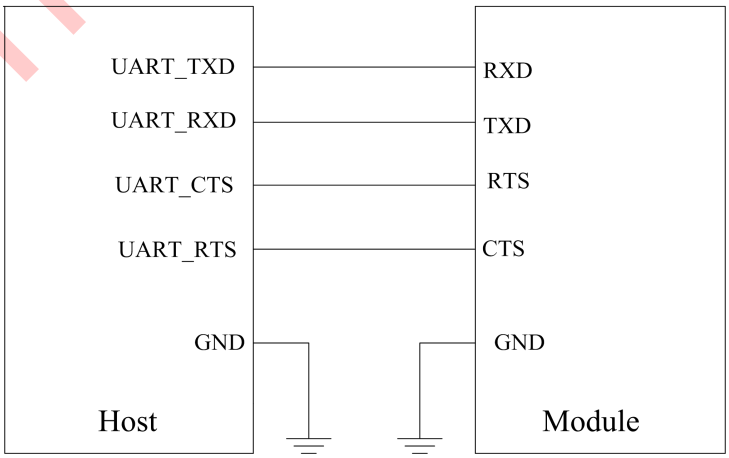


Figure 3-11 UART serial port design

The serial port level of the module is 1.8V. If the serial port needs to be connected to the MCU of 3.3V level, it is necessary to add a level conversion chip externally to achieve level matching. For the chip connection method, refer to the following circuit:

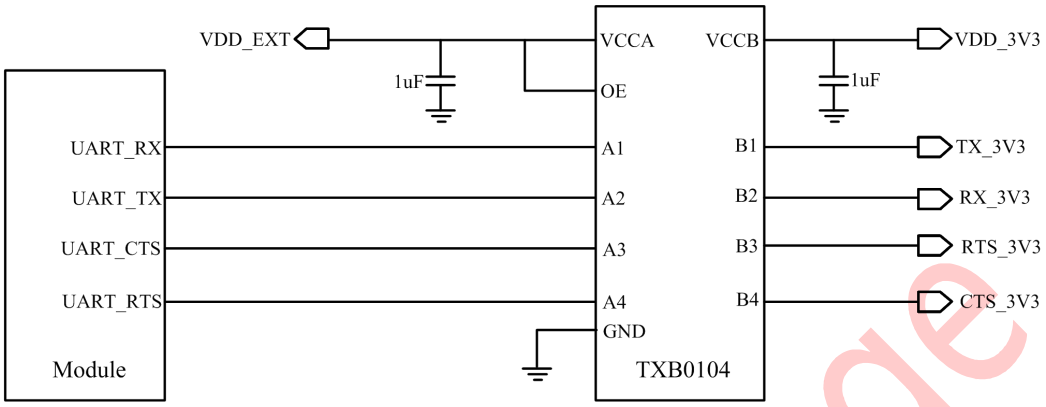


Figure 3-12 Level shifting circuit

3.7 USIM Interface

The CLM920_NC5 Mini PCIE module provides an ISO 7816-3 compliant USIM card interface. The USIM card power supply is provided by the module's internal power regulator and supports 1.8V/3.0V.

Table 3-9 SIM card signal definition

Pin number	Signal name	IO	High value	Description
6	UIM_DET	DI	1.8V	SIM card hot plug detection
8	UIM_PWR	PO	1.8V/2.85V	SIM card power supply
10	UIM_DATA	IO	1.8V/2.85V	SIM card data signal
12	UIM_CLK	DO	1.8V/2.85V	SIM card clock signal
14	UIM_RESET	DO	1.8V/2.85V	SIM card reset signal

3.7.1 USIM Card Reference Circuit

The CLM920_NC5 Mini PCIE module does not come with a USIM card slot. Users need to design a USIM card slot on their own interface board.

The USIM card interface reference design is as follows:

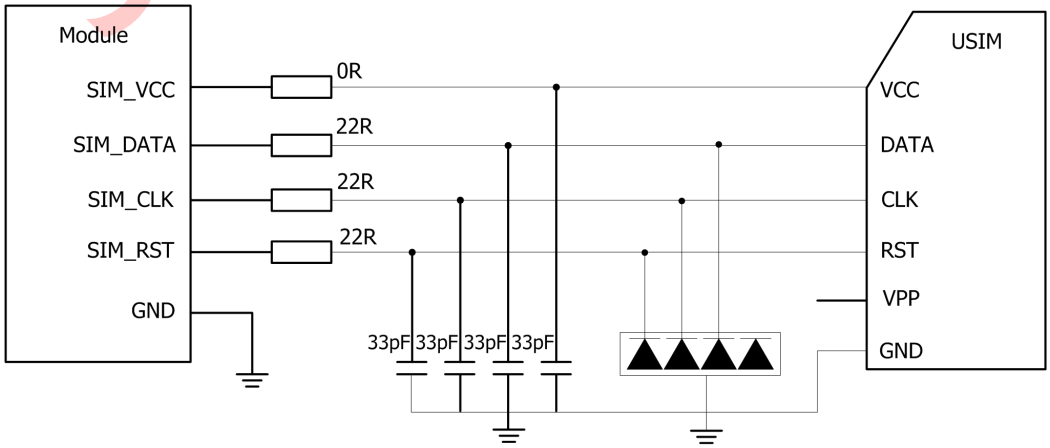


Figure 3-13 USIM design circuit diagram

NOTE

- The USIM interface cable is recommended to use ONSEMI's SMF15C device for ESD protection. The peripheral circuit components should be placed close to the card holder. The SIM card holder is close to the module layout.
- The USIM card circuit is susceptible to radio frequency interference and does not recognize or drop the card. Therefore, the card slot should be placed as far as possible from the RF radiation of the antenna. The card trace should be as far away as possible from the RF, power supply and high-speed signal lines.
- The UIM_DATA has been internally pulled up to VDD_EXT through a 47K resistor, and no external pull-up is required.
- UIM_DET is the USIM card insertion or non-insertion detection pin. It is high by default. The SIM card status can be detected by this PIN pin during hot plug application.
- To avoid transient voltage overload, the USIM interface requires a 22R resistor in series with each other on the signal line path.

3.7.2 USIM_DET Hot Swap Reference Design

The CLM920_NC5 Mini PCIE module supports SIM hot plugging.

The USIM_DET pin acts as an input detection pin to determine whether the SIM card is inserted or not. The UIM_DET pin defaults to a pull-up high.

Table 3-10 SIM card hot swap detection pin definition

NO	UIM_DET status	Functional description
1	High	SIM card insertion, UIM_DET is high
2	Low	SIM card is pulled out, UIM_DET is low

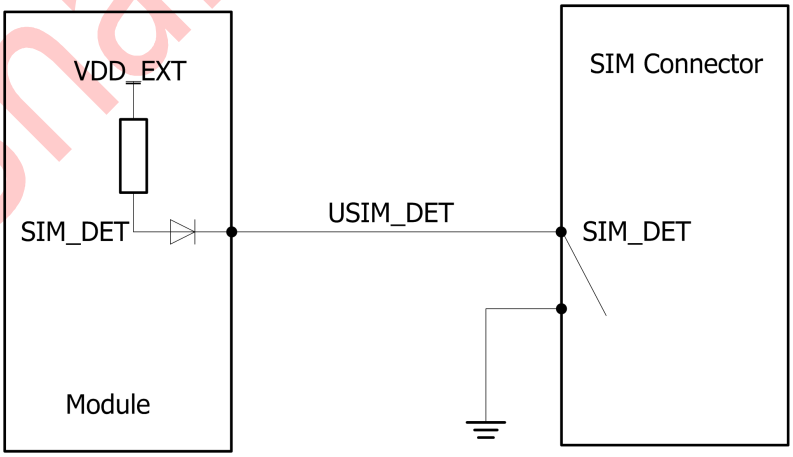


Figure 3-14 SIM card hot plug detection

NOTE

- It is recommended to add a diode protection next to the UIM _DET pin of the module.

✧ When using a normally closed SIM or a normally open SIM card, the detection function can be set by the AT command.

If AT+HOSCFG=1 is set, the status of the SIM card is high when the SIM card is in position, and AT+HOSCFG=1 is set. When the SIM card is in the state, the status is low. Set AT+HOSCFG=0, 0 SIM card hot swap function is off. .

3.8 General GPIO Interface

Table 3-11 General GPIO Pin Definitions

Pin	Signal name	I/O	High value	Description
19	WAKEUP_IN	DI	1.8V	Module sleep control
20	W_DISABLE#	DI	1.8V	Turn off the RF function
32	WAKEUP_OUT	DO		Module wake up host

The CLM920_NC5 Mini PCIE module supports sleep wakeup. WAKEUP_IN wakes up for the host control module sleep, WAKEUP_OUT wakes up the host for the module. When using, you need to set AT^RPTFLAG=0 to enable the wake-up function (you need to set the boot every time).

WAKEUP_IN: This pin is the host wake-up module pin. When the WAKEUP_IN signal is pulled high to 1.8V, the host can wake up the module and pull the module down to enter sleep mode.

WAKEUP_OUT: This pin wakes up the host pin for the module. When there is a voice incoming call or a short message needs to be reported, WAKEUP_OUT will output a rectangular wave to wake up the host.

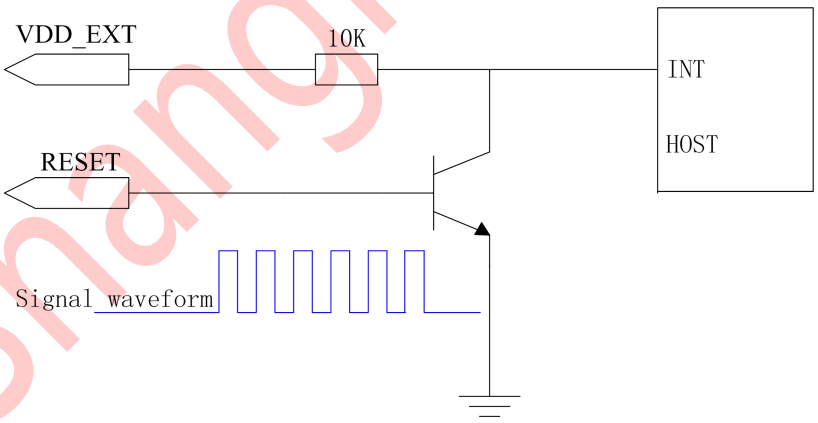


Figure 3-15 WAKEUP_OUT signal waveform

3.9 Network indication interface

The CLM920_NC5 Mini PCIE module provides an open-drain GPIO signal to indicate the status of the RF communication.

Table 3-12 Network indicator pin definition

Pin name	Pin	I/O	Description
LED_WWAN#	42	PI	Network status indicator

Table 3-13 Network indication status

Status	LED display status
No service	Constantly bright
Module registration on non-4G network	Slow flash
The module registers 4G network or module to register non-4G network for voice SMS and other services.	Flashing

The LED network indicator reference design is as follows:

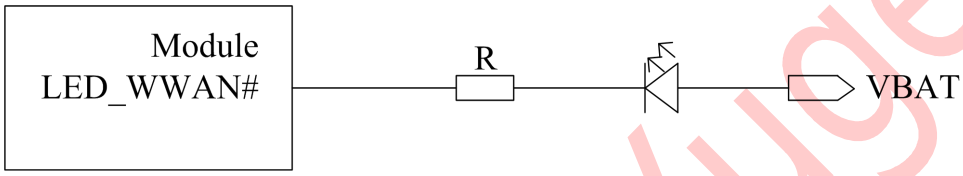


Figure 3-16 Network indicator circuit diagram

NOTE

The brightness of the LED lamp can be adjusted by adjusting the value of the current limiting resistor, and the current can be adjusted to a maximum of 40 mA.

3.10 RF antenna interface

The CLM920_NC5 Mini PCIE module is designed with three antenna interfaces, one main set antenna, one diversity antenna and one GNSS antenna. 4G recommends connecting a diversity antenna to limit high-speed movement and signal degradation caused by multipath.

3.10.1 RF connector position

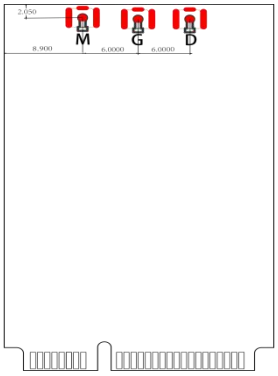


Figure 3-17 Location of the RF connector

3.10.2 RF Connector Size

Customers are advised to use the RF Connector connection method.

- ✧ The antenna connector must use a coaxial connector with a 50 ohm characteristic impedance and use an RF cable with as little insertion loss as possible.
- ✧ Murata's MM9329-2700 connector is recommended.

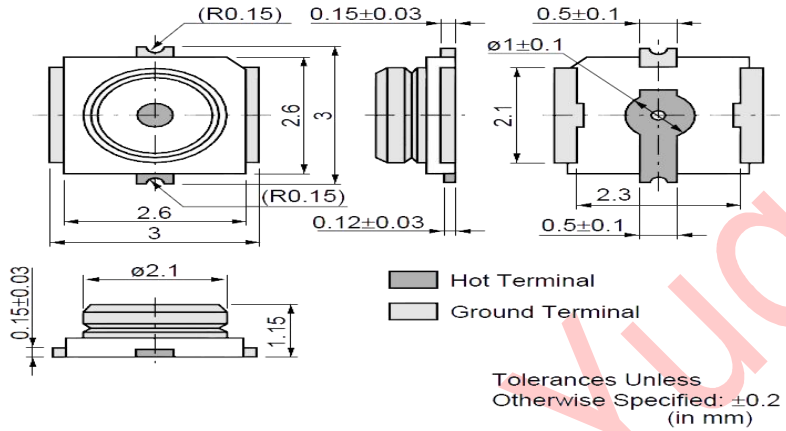


Figure 3-18 RF connector size chart

Table 3-4 Main parameters of the RF connector

Rated condition		Environmental conditions
Frequency Range	DC to 6GHZ	－40° C to +85° C
Characteristic impedance	50 Ω	－40° C to +85° C

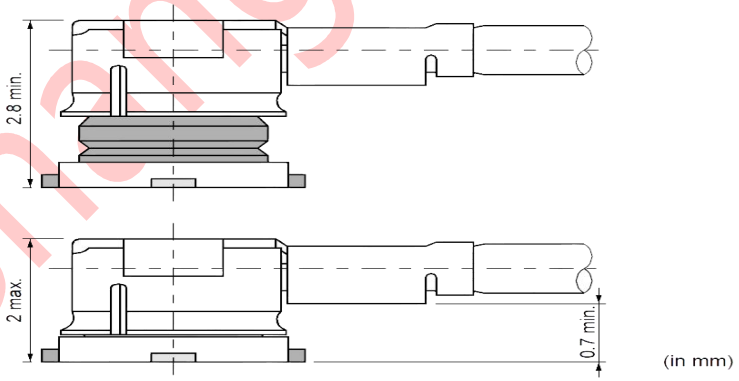


Figure 3-19 Matching coaxial RF line size

NOTE

- ✧ The CLM920_NC5 Mini PCIE module provides three RF antenna interfaces, which are the main set antenna, diversity antenna and GPS antenna (optional). Connected to the antenna must be a 50 ohm characteristic impedance trace.
- ✧ In actual use, the antenna board can be debugged and optimized according to the user's circuit board. The motherboard R1/R2/R3/R4 defaults to 0 ohms, and C1/C2/C3/C4 defaults to empty. During the internal period, it is recommended to attach a bidirectional TVS tube at the antenna connection

D1/D2.

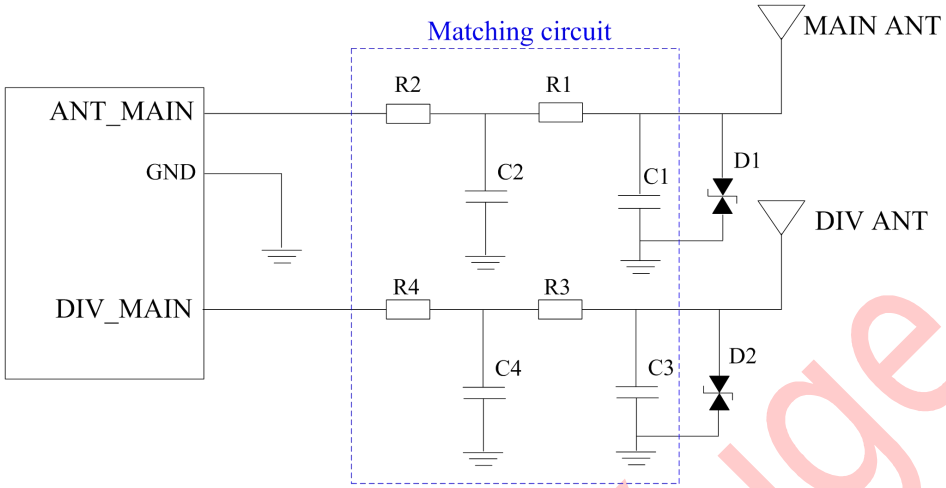


Figure 3-20 Main set and diversity antenna matching circuit

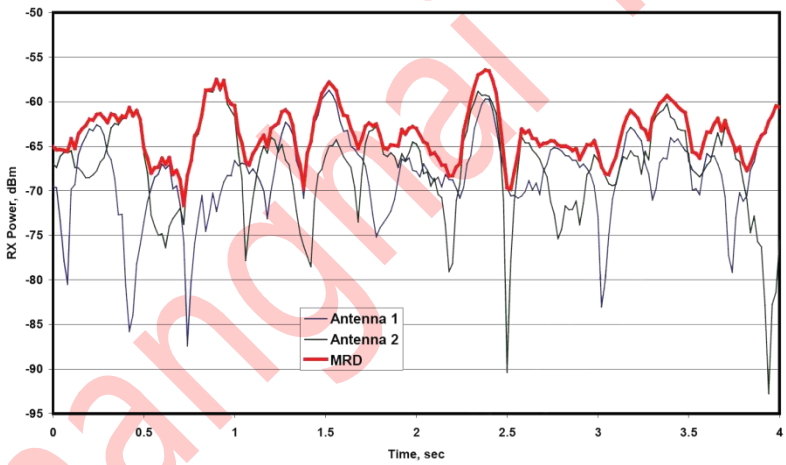


Figure 3-21 Comparison of received signal strengths with and without diversity antennas

3.11 Analog voice interface

The CLM920_NC5 Mini PCIE module provides a set of analog voice interfaces that include one differential input signal (MIC+/MIC-) and one differential output signal SPK+(REC+)/SPK-(REC-).

Table 3-15 Simulation voice pin definition

Pin number	Signal name	I/O	Description
1	MIC+	AI	模拟音频输入+
3	MIC-	AI	模拟音频输入-
5	SPK+/REC+	AO	模拟音频输出+
7	SPK-/REC-	AO	模拟音频输出-

3.11.1 Analog Voice Reference Design

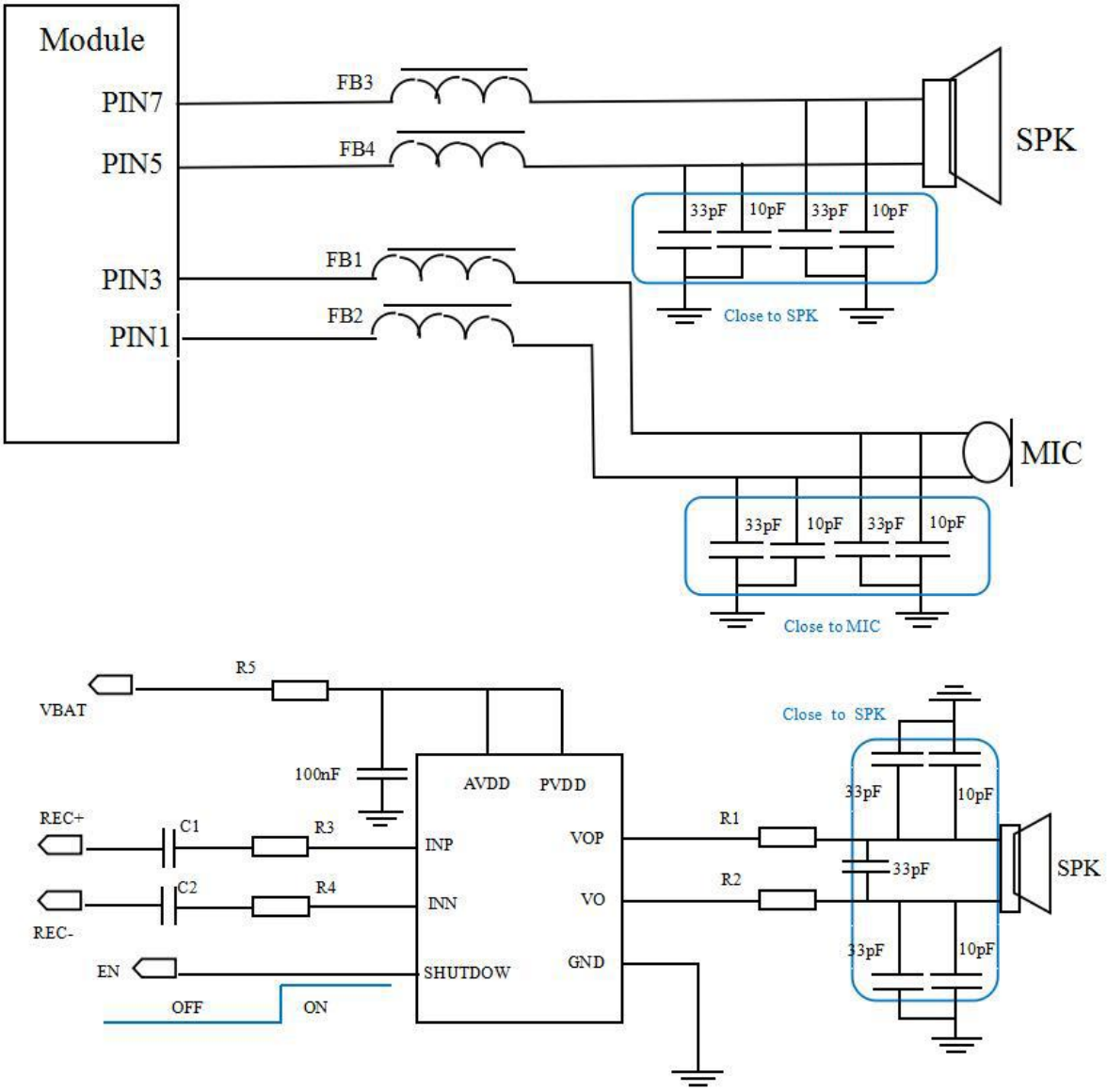


Figure 3-22 Analog voice reference circuit

NOTE

- The MIC+/MIC-channel is used as a differential input for the microphone. The internal bias voltage required for the microphone operation is provided inside the module. No external bias circuit is required. The microphone usually uses an electret microphone.
- The SPK+/SPK-channel is usually used for the handle, earphone or external power amplifier. If the customer needs an external audio amplifier, it will switch to the headphone channel output signal through AT+CSDVC=4, and then the external audio amplifier will amplify the signal.
- The audio signal is sensitive and should be placed away from the radiation source and power interface. The traces should be as short as possible and protect sensitive signals.
- To prevent TDD noise, the filter capacitors are reserved for 10pF and 33pF when designing the audio circuit to remove the RF interference signal.
- The customer can set the handle output by using the AT+CSDVC=4 command, the AT+CSDVC=2

command to set the headphone output; the AT+COUTGAIN command to adjust the handle output volume gain, the AT+CMICGAIN command to set the microphone gain, and the detailed setting information reference to the corresponding AT manual.

3.11.2 PCM digital voice interface

The CLM920_NC5 Mini PCIE module provides a set of PCM audio interfaces supporting 8-bit A-rate, U-rate and 16-bit linear short frame encoding formats with PCM_SYNC of 8kHZ and PCM_CLK of 2048kHZ.

Table 3-16 PCM pin definition

Pin number	Signal name	I/O	description
45	PCM_CLK	DO	PCM clock pulse
47	PCM_DOUT	DO	PCM data output
49	PCM_DIN	DI	PCM data input
51	PCM_SYNC	DO	PCM frame sync signal

Table 3-17 PCM specific parameters

Characteristic	Description
Encoding format	Linear
Data bit	16bits
Master-slave mode	Master/slave mode
PCM clock	2048kHz
PCM frame synchronization	Short frame
Data Format	MSB

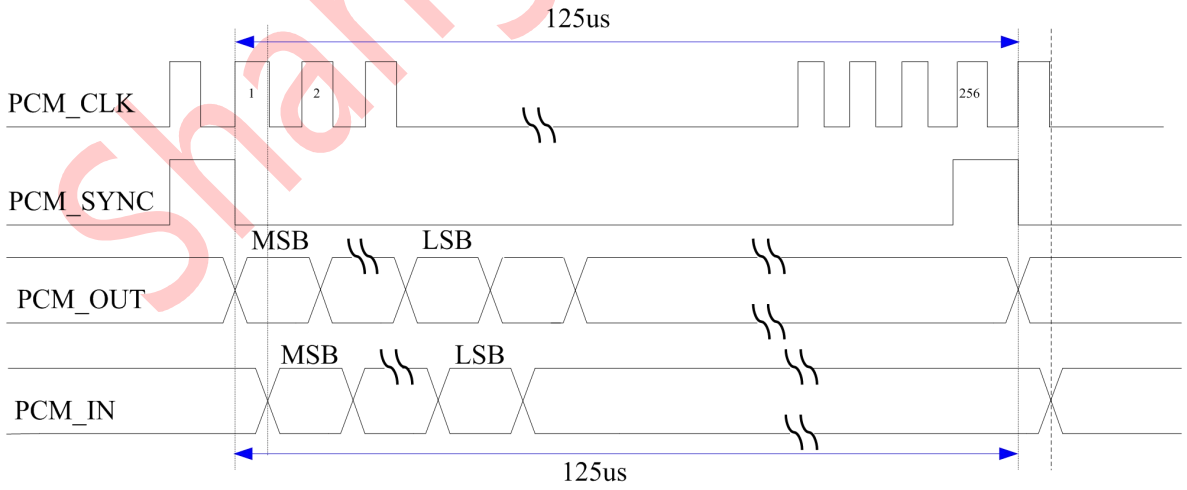


Figure 3-23 PCM short frame mode timing diagram

Chapter 4. Overall technical indicators

4.1 Chapter overview

The CLM920_NC5 Mini PCIE Module RF General Specifications contain the following sections:

- ✧ working frequency;
- ✧ Conducted radio frequency measurement;
- ✧ Conducted receiving sensitivity and transmitting power;

4.2 Working frequency

Table 4-1 RF frequency table

Band	Uplink frequency	Downstream frequency	Duplex mode
LTE B1	1920MHz – 1980MHz	2110MHz – 2170MHz	FDD
LTE B3	1710MHz – 1785MHz	1805MHz – 1880MHz	FDD
LTE B5	824MHz – 849MHz	869MHz – 894MHz	FDD
LTE B7	2500MHz – 2570MHz	2620 MHz – 2690 MHz	FDD
LTE B8	880 MHz – 915 MHz	925 MHz – 960 MHz	FDD
LTE B20	832 MHz – 862 MHz	791 MHz – 821 MHz	FDD
LTE B38	2570MHz – 2620MHz	2570MHz – 2620MHz	TDD
LTE B39	1880MHz – 1920MHz	1880MHz – 1920MHz	TDD
LTE B40	2300MHz – 2400MHz	2300MHz – 2400MHz	TDD

LTE B41	2496MHz - 2690MHz	2496MHz - 2690MHz	TDD
GSM850	824MHz - 849MHz	869MHz - 894MHz	GSM
GSM900	880MHz - 915MHz	925MHz - 960MHz	GSM
DCS1800	1710MHz - 1785MHz	1805MHz - 1880MHz	GSM
UMTS B1	1920MHz - 1980MHz	2110MHz - 2170MHz	WCDMA
UMTS B5	824MHz - 849MHz	869MHz - 894MHz	WCDMA
UMTS B8	880MHz - 915MHz	925MHz - 960MHz	WCDMA
BC0	824MHz - 849MHz	869MHz - 894MHz	CDMA
TDS B34	2010MHz - 2025MHz	2010MHz - 2025MHz	TD-SCDMA
TDS B39	1880MHz - 1920MHz	1880MHz - 1920MHz	TD-SCDMA

4.3 Conducted RF Measurement

4.3.1 Test environment

Table 4-2 Test instruments

Test instrument	Power supply	Murata coaxial RF line
R&S CMW500	Agilent 66319	MXHP32HP1000

4.3.2 Test Standards

The CLM920_NC5 Mini PCIE module passes the 3GPP TS 51.010-1, 3GPP TS 34.121-1, 3GPP TS 36.521-1, 3GPP2 C.S0011 and 3GPP2 C.S0033 test standards. Each module is rigorously tested at the factory to ensure reliable quality.

4.4 Conducted Receive Sensitivity and Transmit Power

CLM920_NC5 Mini PCIE module 2G and 3G receiving sensitivity and transmit power test indicators are as follows:

Table 4-3 2G3G RF indicators

Mode	Upstream	Down	Power	Receiving sensitivity
GSM 850	824MHz - 849MHz	869MHz - 894MHz	33±2dBm	<-109dBm
GSM 900	880MHz - 915MHz	925MHz - 960MHz	33±2dBm	<-109dBm
DCS 1800	1710MHz-1785MHz	1805MHz - 1880MHz	30±2dBm	<-109dBm
WCDMA B1	1920MHz-1980MHz	2110MHz - 2170MHz	23+2/-2dBm	<-109dBm
WCDMA B5	824MHz - 849MHz	869MHz - 894MHz	23+2/-2dBm	<-109dBm
WCDMA B8	880MHz -	925MHz -	23+2/-2dBm	<-109dBm

	915MHz	960MHz		
TD-SCDMA B34	2010MHz-2025MHz	2010MHz－2025MHz	24+1/-3dBm	<-109dBm
TD-SCDMA B39	1880MHz-1920MHz	1880MHz－1920MHz	24+1/-3dBm	<-109dBm
EVDOrA	824MHz－849MHz	869MHz－894MHz	23+2/-2dBm	<-108dBm

CLM920_NC5 Mini PCIE module 4G receiving sensitivity and transmit power test indicators are as follows:

Table 4-4 4G RF sensitivity indicators

Directory (sensitivity)	3GPP protocol requirements	Min	Typical	Max
LTE B1（FDD QPSK 通过）95%）	< －96.3(10 MHz)		-99	-98
LTE B3（FDD QPSK 通过）95%）	< －93.3(10 MHz)		-96	-95
LTE B5（FDD QPSK 通过）95%）	< －94.3(10 MHz)		-97	-96
LTE B7（TDD QPSK 通过）95%）	< －94.3(10 MHz)		-97	-96
LTE B8（TDD QPSK 通过）95%）	< －93.3(10 MHz)		-97	-96
LTE B20（TDD QPSK 通过）95%）	< －93.3(10 MHz)		-96	-95
LTE B38（TDD QPSK 通过）95%）	< －96.3(10 MHz)		-98	-97
LTE B39（TDD QPSK 通过）95%）	< －96.3(10 MHz)		-99	-98
LTE B40（TDD QPSK 通过）95%）	< －96.3(10 MHz)		-99	-98
LTE B41（TDD QPSK 通过）95%）	< －96.3(10 MHz)		-98	-97

Table 4-5 4G RF transmit power indicators

Directory	3GPP Protocol Requirements (dBm)	Min	Typical	Maximum
LTE B1	21 to 25	22	23	24
LTE B3	21 to 25	22	23	24
LTE B5	21 to 25	22	23	24
LTE B7	21 to 25	22	23	24
LTE B8	21 to 25	22	23	24
LTE B20	21 to 25	22	23	24
LTE B38	21 to 25	22	23	24
LTE B39	21 to 25	22	23	24
LTE B40	21 to 25	22	23	24
LTE B41	21 to 25	22	23	24

4.5 Antenna requirements

CLM920_NC5 Mini PCIE module main set antenna and GNSS antenna design requirements:

Table 4- 6 Main set antenna indicator requirements

Band	Standing wave ratio	Antenna gain	Effectiveness	TRP	TIS
GSM850	<2.5:1	〉-4dbi	〉40%	29	<-102
GSM900	<2.5:1	〉-4dbi	〉40%	29	<-102
DCS1800	<2.5:1	〉-4dbi	〉40%	26	<-102
B1 FDD	<2.5:1	〉-4dbi	〉40%	19	<-94
B3 FDD	<2.5:1	〉-4dbi	〉40%	19	<-91
B5 FDD	<2.5:1	〉-4dbi	〉40%	19	<-92
B7 FDD	<2.5:1	〉-4dbi	〉40%	19	<-92
B8 FDD	<2.5:1	〉-4dbi	〉40%	19	<-94
B20 FDD	<2.5:1	〉-4dbi	〉40%	19	<-94
B38 TDD	<2.5:1	〉-4dbi	〉40%	19	<-93
B39 TDD	<2.5:1	〉-4dbi	〉40%	19	<-93
B40 TDD	<2.5:1	〉-4dbi	〉40%	19	<-93
B41 TDD	<2.5:1	〉-4dbi	〉40%	19	<-93
WCDMA B1	<2.5:1	〉-4dbi	〉40%	19	<-106
WCDMA B5	<2.5:1	〉-4dbi	〉40%	19	<-106
WCDMA B8	<2.5:1	〉-4dbi	〉40%	19	<-106
EVDOrA	<2.5:1	〉-4dbi	〉40%	19	<-106
B34 TDS	<2.5:1	〉-4dbi	〉40%	19	<-106
B39 TDS	<2.5:1	〉-4dbi	〉40%	19	<-106

Table 4-7 GNSS antenna indicator requirements

Frequency band	Standing wave ratio	Active noise figure	Active gain	Active antenna embedded gain
GPS L1 1575.41+/1.023MHZ	<2:1	<1.5DB	>-2DBi	20DB
GLONASS 1597.5-1605.8MHZ	<2:1	<1.5DB	>-2DBi	20DB
BeiDou 1559.05-1563.14MHZ	<2:1	<1.5DB	>-2DBi	20DB

4.6 Power Consumption Characteristics

Table 4-8 GSM power consumption

Frequency band	Configuration	Power level	Current consumption (mA)
GPRS850	1UP/1DL	5	310
GPRS900	1UP/1DL	5	315
GPRS1800	1UP/1DL	0	200
EDGE850	1UP/1DL	8	220
EDGE900	1UP/1DL	8	225
EDGE1800	1UP/1DL	2	175

Table 4-9 WCDMA Power Consumption

Frequency band	Power (dbm)	Current consumption (mA)
WCDMA B1	23.2	556
WCDMA B1	1	165
WCDMA B5	22.6	590
WCDMA B5	1	152
WCDMA B8	22.4	532
WCDMA B8	1	144

Table 4-10 LTE power consumption

Frequency band	Power (dbm)	Current consumption (mA)
B1	21.5	562
B3	21.8	590
B5	22.5	575
B7	22.1	597
B8	23.2	562
B20	23.5	571
B38	22.5	465
B39	21.9	375
B40	22.1	362
B41	22.8	482

Table 4-11 TDS-CDMA power consumption

Frequency band	Power (dbm)	Current consumption (mA)
TDS B34	22.8	173
TDS B39	23.1	180

Chapter 5. Interface electrical characteristics

5.1 Working storage temperature

Table 5-1 CLM920_NC5 4G module operating temperature

Parameter	Minimum	Maximum
Normal operating temperature	-35° C	75° C
Extreme working temperature	-40° C	85° C

5.2 Module IO Level

CLM920_NC5 Mini PCIE module IO level is as follows:

The corresponding UIM_PWR is 1.8V for the 1.8V USIM application. The UIM_PWR is 2.85V for the 3V USIM application.

Other digital IO levels are unified to 1.8V.

Table 5-2 Electrical characteristics of the CLM920_NC5 Mini PCIE module

Parameter	Parameter Description	Minimum	Maximum
VIH	High level input voltage	0.65* VDD_EXT	VDD_EXT+0.3V
VIL	Low level input voltage	-	0.35*VDD_EXT
VOH	High level output voltage	VDD_EXT-0.45V	VDD_EXT
VOL	Low level output voltage	0	0.45V

5.3 Power supply

The input power requirements of the CLM920_NC5 Mini PCIE module are as follows:

Table 5-3 CLM920_NC5 module working voltage

Parameter	Minimum	Typical	Maximum
VBAT	3.3V	3.7V	4.2V
UIM_PWR	1.7V/2.75V	1.8V/2.85V	1.9V/2.95V

The power-on time of any interface of the module must not be earlier than the boot time of the module. Otherwise, the module may be abnormal or damaged.

5.4 Electrostatic property

The CLM920_NC5 Mini PCIE module requires ESD protection to ensure product quality.

Table 5-4 CLM920_NC5 ESD Features

Test port	Contact discharge	Air discharge	Unit
USB interface	±4	±8	KV
USIM interface	±4	±8	KV
Analog voice interface	±4	±8	KV
VBAT power supply	±4	±8	KV

Chapter 6. Structural and mechanical properties

6.1 Appearance

The CLM920_NC5 Mini PCIE module is a single-sided PCBA. The appearance of the module is as follows:

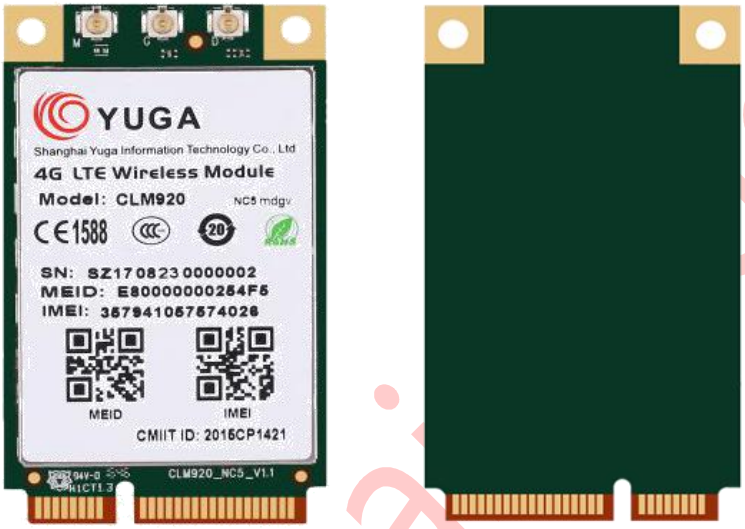


Figure 6-1 Appearance of the CLM920_NC5

6.2 Mini PCI Express Connector

The CLM920_NC5 Mini PCIE module interface complies with the PCI Express Mini Card 1.2 interface standard.PCI Express Mini Card connectors that meet this standard can be used with them, such as Molex's 679100002.

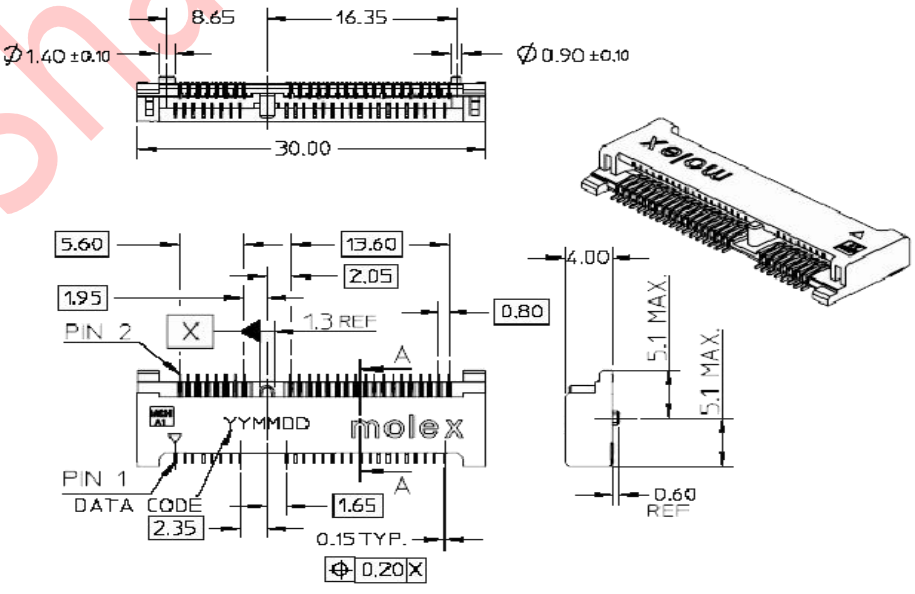


Figure 6-2 Connector dimensions

6.3 Module fixing method

The CLM920_NC5 Mini PCIE module is fixed in two screw holes.