Product name	CLM920_AC3 Module Hardware Usage Guide
Number of pages	59
Version	V1.0
Date	2019/3/21

CLM920_AC3
Module Hardware Usage Guide

V1.0

Shanghai Yuge Information Technology co., LTD

Revise history

Version	Date	Description	Author
V1.0	20190321	Initialized version	David

Contents

Image index

Table index

Chapter 1. Introduction

This document is a hardware solution manual for the wireless solution product CLM920 AC3 module. It is intended to describe the hardware components and functional characteristics of the module solution, application interface definition and usage instructions, electrical performance and mechanical characteristics. Combined with this and other application documents, users can quickly use this module to design wireless products.

Chapter 2. Module Overview

2.1 Module introduction

The CLM920_AC3 module is a wireless communication module that integrates various network standards such as FDD-LTE/TDD-LTE/WCDMA, and supports a maximum downlink rate of 150 Mbps and a maximum uplink rate of 50 Mbps. The module is based on ASR's ASR1802SL platform. It has built-in multiple network protocols (PAP, PPP, CHAP, TCP, UDP, etc.) and supports multiple functions (WAKEUP, W_DISABLE, AP_READY, etc.), and supports Windows 7/Windows 8/Windows 10/. Embedded operating system such as Android 4.0 or higher.

The CLM920 AC3 module can be used in the following applications:

- ✧ Car Equipment
- ✧ Wireless POS machine
- ✧ Wireless advertising, multimedia
- ✧ Remote monitoring
- ✧ Smart meter reading
- ✧ Mobile broadband
- ✧ automated industry
- ✧ Other wireless terminals, etc.

2.2 Module characteristics

Table 2-1 Key Features

Characteristic		Description
Physical characteristics		32mm x 29mm x 2.4mm
Fixed way		LCC package, patch mount
Operating Voltage		3.3V - 4.2V Typical Voltage 3.7V
Energy saving current		Standby current < 5mA
	USIM card interface	Support 3.0V/1.8V, support hot swap function
	USB interface	✧ USB2.0 (High-Speed) (only supports slave mode), data transfer rate up to 480Mbps ✧ For AT commands, data transfer, software debugging and software upgrades

应用接口		✧ USB driver: Supports Windows XP, Windows 7, Windows 10, Windows CE 5.0/6.0/7.0, Linux 2.6 or higher ✧ Android 2.3/4.0/4.2/4.4/5.0/6.0/7.1, etc.
	UART interface	✧ Main serial port (4 lines): ✧ Support RTS and CTS hardware flow control ✧ For AT commands and data transfer ✧ The baud rate is up to 921600bps and the default is 115200bps. ✧ Debug serial port (2 lines): ✧ Used for debugging information output, printing module logs ✧ The default baud rate is 115200bps
	PCM interface	✧ For audio, external codec chip ✧ Supports 8-bit A-law, U-law and 16-bit linear encoding formats ✧ Support short frame mode ✧ Support main mode
	SDIO interface	✧ External WLAN chip, interface voltage 1.8V. ✧ Compliant with SDIO 3.0 protocol ✧ Comply with IEEE 802.11 standard
	I2C interface	✧ Compliant with I2C bus protocol ✧ High speed mode supports 3.3Mbps rate
	ADC interface	✧ Supports two 12-bit sampling ADCs, ✧ Voltage input range 0~1.3V
	Network indication	✧ NET_STATUS network status indication ✧ NET_MODE network registration status indication ✧ STATUS module operating status indication
	General purpose GPIO	✧ WAKEUP_IN sleep mode control, low level wake-up module ✧ AP_READY sleep state detection ✧ W_DISABLE# flight mode control
Frequency band		✧ LTE-TDD:B34/B38/B39/B40/B41 ✧ LTE-FDD:B1/B3/B5/B8

	✧ WCDMA:B1/B5/B8
Transmit power	✧ LTE: Class 3(23dBm±2dB) ✧ UMTS: Class 3(24dBm+1/-3dB)
Data service	✧ WCDMA(3GPP R8) UMTS R99: DL 384kbps/UL 384kbps DC-HSPA+: DL 42Mbps/UL 5.76Mbps ✧ LTE(non-CA Cat4) LTE FDD:DL 150Mbps/UL 50Mbps@20M BW cat4 LTE TDD:DL 130Mbps/UL 35Mbps@20M BW cat4
AT command	✧ Support for standard AT instruction sets (Hayes 3GPP TS 27.007 and 27.005) ✧ Specific AT query CLM920 AC3 AT command set
Network protocol	Support TCP/UDP/PPP/HTTP/NITZ/CMUX/NDIS/NTP/ HTTPS/PING protocol
Antenna interface	✧ MAIN×1，DIV×1 ✧ Characteristic impedance 50 Ω
Virtual network card	✧ Support USB virtual network card
Temperature range	✧ Normal operating temperature -30 ° C to +75 ° C ✧ Extreme operating temperature -40° C to +85° C
Storage temperature	✧ -40° C to +85° C
Humidity	✧ RH5%～RH95%
Module function distinction	✧ M on the label paper represents the main set, D-band table diversity

NOTE

When the temperature is in the range of －40° C to －30° C or +75° C to +85° C, some RF indicators of the CLM920 AC3 module may exceed the 3GPP standard by the 3GPP standard.

2.3 Module function

The CLM920 AC3 LCC module mainly consists of the following circuit units:

✧ Baseband processing unit

✧ Power management unit

- ✧ Memory unit
- ✧ RF transceiver unit
- ✧ Module interface unit

The functional block diagram of the CLM920 AC3 LCC module is shown below：

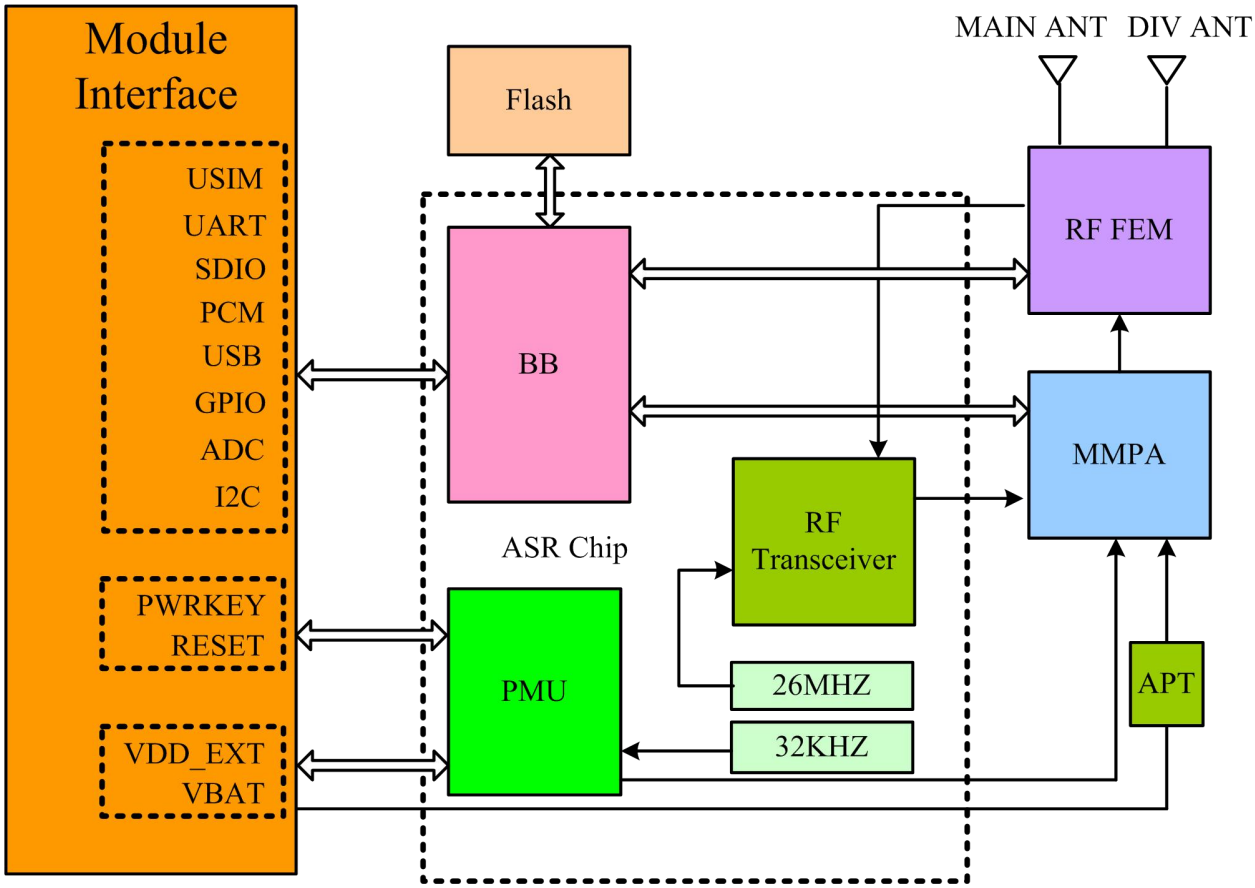

Figure 2-1 Functional block diagram of the CLM920 AC3 LCC module

Chapter 3. Interface Application Description

3.1 Chapter overview

This chapter mainly describes the interface definition and application of this module.

Contains the following sections:

- ✧ 144 pin pin distribution map
- ✧ Interface definition
- ✧ Power interface
- ✧ USB interface
- ✧ USIM interface
- ✧ UART interface
- ✧ ADC interface
- ✧ Status indication interface
- ✧ PCM digital voice interface
- ✧ GPIO interface
- ✧ WLAN interface
- ✧ RF antenna interface

3.2 Module interface

3.2.1 Module pin distribution

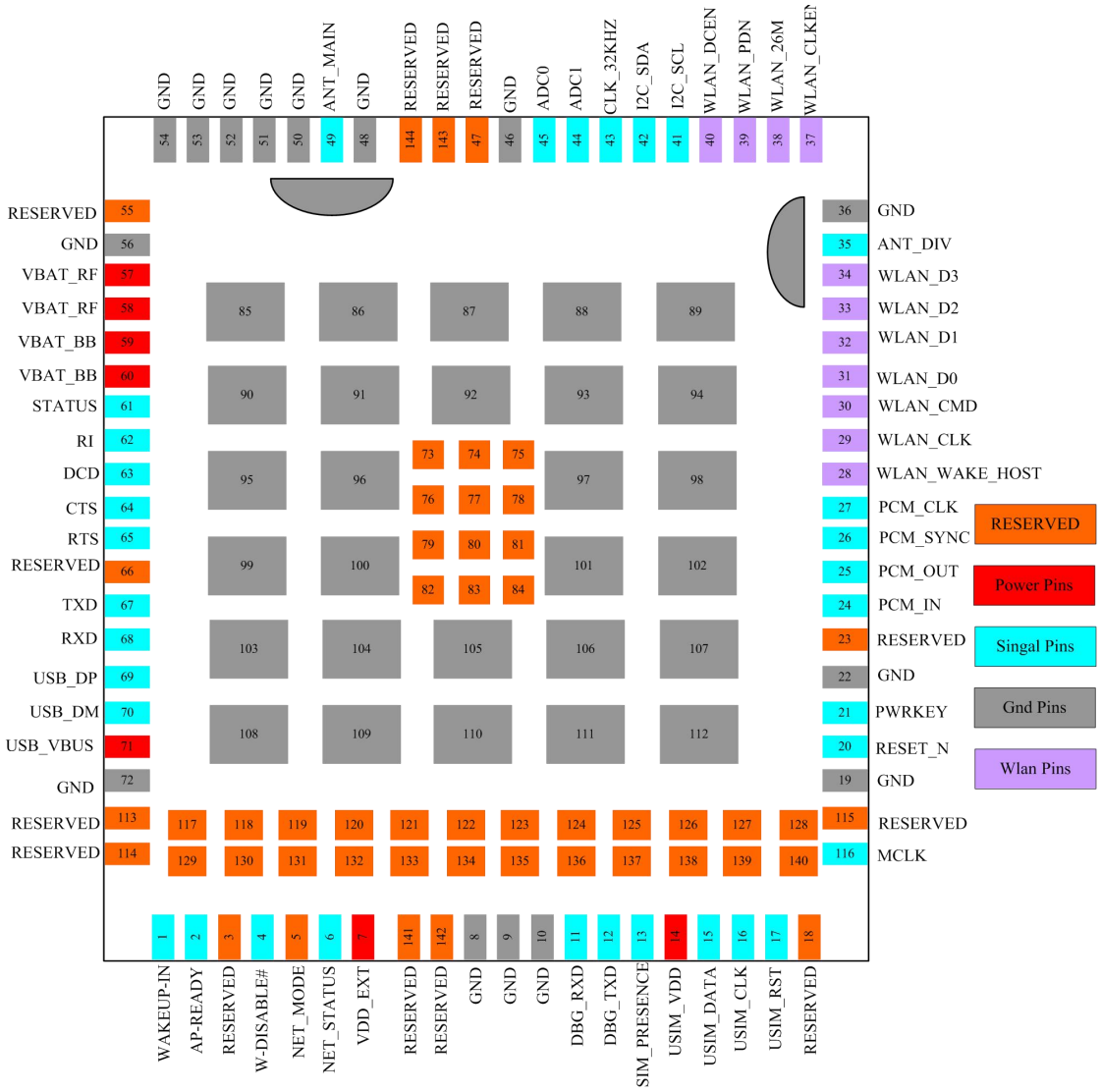

Figure 3-1 CLM920_AC3 module pin distribution diagram (TOP surface perspective)

NOTE

- ✧ The modules Pin85~Pin112 are heat-dissipating pads. It is recommended to ground the design during design.
- ✧ All RESERVED and unused Pin feet need to be left floating.
- ✧ Modules Pin28~Pin34 and Pin37~Pin40 are WLAN function pins. This function is currently under development.

3.2.2 Pin definition

The CLM920_AC3 module is an LCC interface module. Its pin definitions are shown in the following table：

Table 3-1 Pin definitions

Pin	Pin name	Pin	Pin name
1	WAKEUP_IN	2	AP_READY
3	RESERVED	4	W_DISABLE#
5	NET_MODE	6	NET_STATUS
7	VDD_EXT	8	GND
9	GND	10	GND
11	DBG_RXD	12	DBG_TXD
13	SIM_PRESENCE	14	USIM_VDD
15	USIM_DATA	16	USIM_CLK
17	USIM_RST	18	RESERVED
19	GND	20	RESET_N
21	PWRKEY	22	GND
23	RESERVED	24	PCM_IN
25	PCM_OUT	26	PCM_SYNC
27	PCM_CLK	28	WLAN_WAKE_HOST
29	WLAN_CLK	30	WLAN_CMD
31	SDC_DATA0	32	SDC_DATA1
33	SDC_DATA2	34	SDC_DATA3
35	ANT_DIV	36	GND
37	WLAN_CLK_EN	38	WLAN_CLK_26M
39	WLAN_PDN	40	WLAN_DCEN
41	I2C_SCL	42	I2C_SDA
43	CLK_32K	44	ADC1
45	ADC0	46	GND
47	RESERVED	48	GND
49	ANT_MAIN	50	GND
51	GND	52	GND

53	GND	54	GND
55	RESERVED	56	GND
57	VBAT_RF	58	VBAT_RF
59	VBAT_BB	60	VBAT_BB
61	STATUS	62	RI
63	DCD	64	CTS
65	RTS	66	RESERVED
67	TXD	68	RXD
69	USB_DP	70	USB_DM
71	USB_VBUS	72	GND
73	RESERVED	74	RESERVED
75	RESERVED	76	RESERVED
77	RESERVED	78	RESERVED
79	RESERVED	80	RESERVED
81	RESERVED	82	RESERVED
83	RESERVED	84	RESERVED
85	GND	86	GND
87	GND	88	GND
89	GND	90	GND
91	GND	92	GND
93	GND	94	GND
95	GND	96	GND
97	GND	98	GND
99	GND	100	GND
101	GND	102	GND
103	GND	104	GND
105	GND	106	GND
107	GND	108	GND
109	GND	110	GND
111	GND	112	GND
113	RESERVED	114	RESERVED
115	RESERVED	116	RESERVED

117	RESERVED	118	RESERVED
119	RESERVED	120	RESERVED
121	RESERVED	122	RESERVED
123	RESERVED	124	RESERVED
125	RESERVED	126	RESERVED
127	RESERVED	128	RESERVED
129	RESERVED	130	RESERVED
131	RESERVED	132	RESERVED
133	RESERVED	134	RESERVED
135	RESERVED	136	RESERVED
137	RESERVED	138	RESERVED
139	RESERVED	140	RESERVED
141	RESERVED	142	RESERVED
143	RESERVED	144	RESERVED

Table 3-2 IO parameter definition

Symbol sign	**Description**
IO	Two-way input and output
PI	Power input
PO	Power Output
AI	Analog input
AO	Analog output
DI	Digital input
DO	Digital output
OD	Leaky open circuit

Table 3-3 Pin description

Power supply				
Pin	**Definition**	**IO**	**Functional description**	**Remarks**
57	VBAT_RF	PI	Module RF power input	Power supply needs to guarantee 2A current
58	VBAT_RF	PI	Module RF power input	
59	VBAT_BB	PI	Module baseband power input	

60	VBAT_BB	PI	Module baseband power input	
7	VDD_EXT	PO	1.8V voltage output	Can provide pull-up for external GPIO (maximum 50MA), please keep left floating
8~10,19,22, 36,46,48,50 ~54,56,72	GND		Ground	
85~112	GND		Heat sink pad	
Module switch machine and reset				
Pin	**Definition**	**IO**	**Functional description**	**Remarks**
21	PWRKEY	DI	Switching machine pin	Default low active
20	RESET_N	DI	Module reset pin, internally pulled up to VDD_EXT	Low level reset module
USB interface				
Pin	**Definition**	**IO**	**Functional description**	**Remarks**
71	USB_VBUS	PI	USB insertion detection	
69	USB_D+	IO	USB bus differential positive signal	90 Ω differential impedance
70	USB_D-	IO	USB bus differential negative signal	90 Ω differential impedance
Main serial port				
Pin	**Definition**	**IO**	**Functional description**	**Remarks**
62	RI	DO	Ringing prompt	Wake up the host, please keep it floating when not in use
63	DCD	DO	Carrier detection	1.8V, please hang when not in use
64	CTS	DO	Clear send	1.8V, please hang when not in use

65	RTS	DI	Request to send	1.8V, please hang when not in use
67	TXD	DO	Main serial port data transmission	1.8V, please hang when not in use
68	RXD	DI	Main serial data reception	1.8V, please hang when not in use
Debug serial port				
Pin	**Definition**	**IO**	**Functional description**	**Remarks**
11	DBG_RXD	DI	Debug serial port data reception	1.8V, please hang when not in use
12	DBG_TXD	DO	Debug serial port data transmission	1.8V, please hang when not in use
USIM interface				
Pin	**Definition**	**IO**	**Functional description**	**Remarks**
13	SIM_PRESENCE	DI	USIM card hot plug detection	please hang when not in use
14	USIM_VDD	PO	USIM card power supply	Automatically recognize 1.8V or 3V USIM cards
15	USIM_DATA	IO	USIM card data signal line	
16	USIM_CLK	DO	USIM card clock signal line	
17	USIM_RST	DO	USIM card reset signal line	
GPIO pin				
Pin	**Definition**	**IO**	**Functional description**	**Remarks**
1	WAKEUP_IN	DI	External device wake-up module	1.8V voltage domain
2	AP_READY	DO	Wake up external devices	Reserved
4	W_DISABLE#	DI	Flight mode control	Pin function is under development (floating when not in use)
Module status indication interface				

Pin	Definition	IO	Functional description	Remarks
5	NET_MODE	DO	Module 4G Network Status Indicator	1.8V, please hang when not in use
6	NET_STATUS	DO	Module network status indication	1.8V, please hang when not in use
61	STATUS	DO	Module running status indication	1.8V, please hang when not in use
PCM interface				
Pin	**Definition**	**IO**	**Functional description**	**Remarks**
24	PCM_IN	DI	PCM receiving data	1.8V voltage domain
25	PCM_OUT	DO	PCM sends data	1.8V voltage domain
26	PCM_SYNC	IO	PCM frame sync signal	1.8V voltage domain
27	PCM_CLK	IO	PCM clock pulse	1.8V voltage domain
I2C interface				
Pin	**Definition**	**IO**	**Functional description**	**Remarks**
41	SCL	DO	I2C bus clock	Internal 4.7K pull-up
42	SDA	IO	I2C bus data	Internal 4.7K pull-up
WLAN interface				
Pin	**Definition**	**IO**	**Functional description**	**Remarks**
28	WLAN_WAKE_HOST	DI	**HOST to SOC wakeup**	
29	SDC_CLK	IO	SDIO bus clock output	Keep empty when not in use
30	SDC_CMD	IO	SDIO bus command output	Keep empty when not in use
31	SDC_D0	IO	SDIO bus DATA0	Keep empty when not in use
32	SDC_D1	IO	SDIO bus DATA1	Keep empty when not in use
33	SDC_D2	IO	SDIO bus DATA2	Keep empty when not in use
34	SDC_D3	IO	SDIO bus DATA3	Output

				configurable, no need
37	WLAN_CLK_EN	DO	OSC mode enable	
38	WLAN_CLK_26M		26M clock	External 26M clock
39	WLAN_PDN	DO	WLAN power down mode	Active low
40	WLAN_DCEN	DO	External LDO enable control	Active high
ADC interface				
Pin	**Definition**	**IO**	**Functional description**	**Remarks**
44	ADC1	AI	12bits resolution universal analog to digital conversion	Input range 0~1.3V
45	ADC0	AI	12bits resolution universal analog to digital conversion	Input range 0~1.3V
RF interface				
Pin	**Definition**	**IO**	**Functional description**	**Remarks**
35	ANT_DIV	AI	Diversity antenna	50 Ω characteristic impedance
49	ANT_MAIN	IO	Main antenna	50 Ω characteristic impedance

RESERVED interface			
Pin	**Definition**	**Functional description**	**Remarks**
3，18，23，43，47，55，66，73~84，113~144	RESERVED	Reserved pin	Please stay vacant

NOTE

- ✧ The module typically has an IO port level of 1.8V (in addition to the SIM, the SIM card port level supports 1.8V and 3.0V).
- ✧ This module defines the RESERVED pin as a reserved pin. It is recommended to be suspended and must not be used.。

3.3 Power interface

The CLM920 AC3 module power connector consists of three parts:

- ✧ VBAT_BB, VBAT_RF is the module working power supply
- ✧ USIM_VDD is the working power supply for SIM card
- ✧ VDD_EXT is 1.8V output power (50mA)

3.3.1 Power supply design

CLM920 AC3 module power interface is as follows：

Table 3-4 Power pin definitions

Pin	Name	I/O	Description	Min	Typical	Max
57,58	VBAT_RF	PI	Module power supply	3.3V	3.7V	4.2V
59,60	VBAT_BB	PI	Module power supply	3.3V	3.7V	4.2V
14	USIM_VDD	PO	SIM card power supply	0	1.8V/2.85V	1.98/3.3V
7	VDD_EXT	PO	LDO output		1.8V	
8~10,19,22,36,46,48,50~54,56,72, 85~112	GND		Ground	-	0	-

The CLM920 AC3 module is powered by a single power supply and the module provides four power supply pins. Two of them are RF power supplies and two are baseband power supplies. The power supply range is from 3.3V to 4.2V. It is recommended to use 3.7V/2A power supply. If the module's operating voltage drop causes the VBAT supply voltage to be too low or the supply current is insufficient, the module may shut down or restart. Therefore, in order to reduce the power fluctuation of the module when working, it is necessary to use a low-ESR value of the voltage regulator capacitor, the power pin and the ground pin should be connected and can provide sufficient power supply capability.

Under the premise of ensuring that the VBAT power supply is sufficient, two 470uF/6.3V tantalum capacitors can be connected in parallel with the power input, 1uF in parallel, 0.1uF

capacitor (eliminating clock and digital signal interference) and 10pF, 33pF (eliminating low frequency RF interference). Ceramic capacitors.

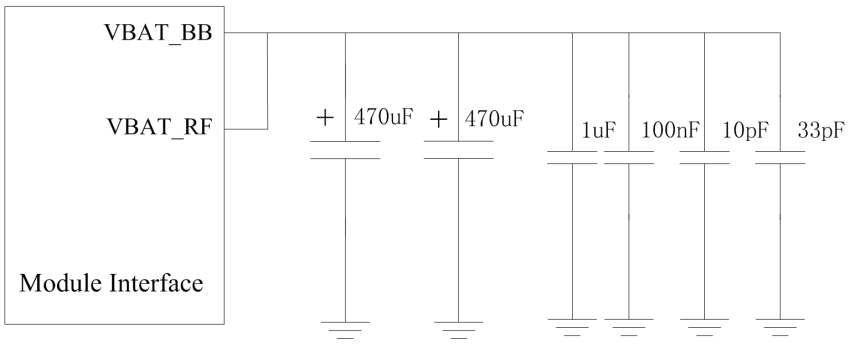

Figure 3-2 Power supply design

3.3.2 Power reference circuit

In actual design, the power circuit can be designed using a switching DC power supply or a linear LDO power supply, and then the PMOS transistor is used to control the power supply input so that the power supply can be completely cut off. Both design circuits need to supply enough current. Specific reference to the following circuit design.

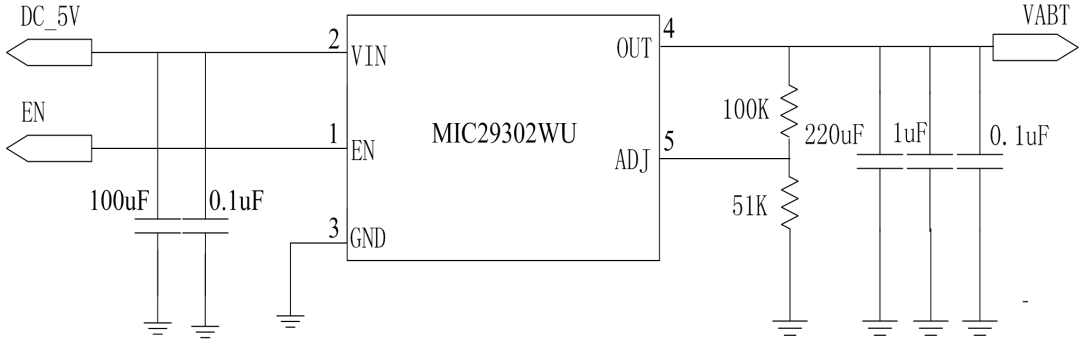

Figure 3-3 LDO linear power supply reference circuit

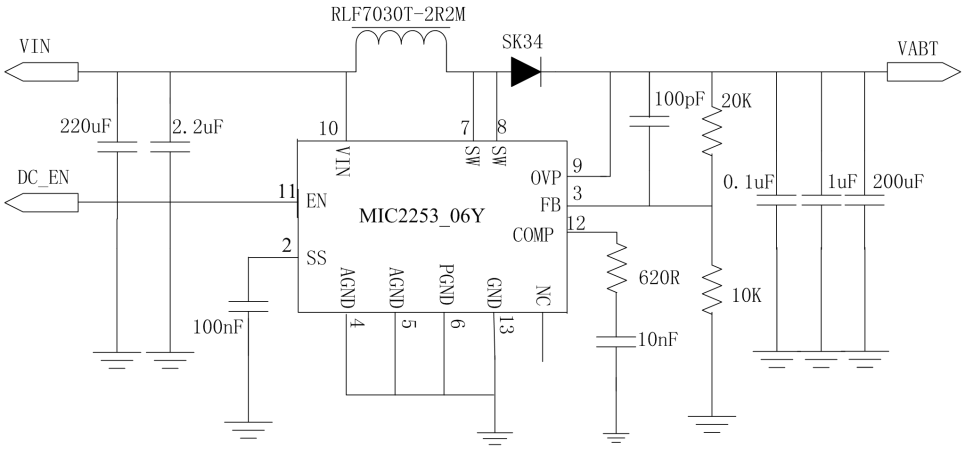

Figure 3-4 DC switching power supply reference circuit

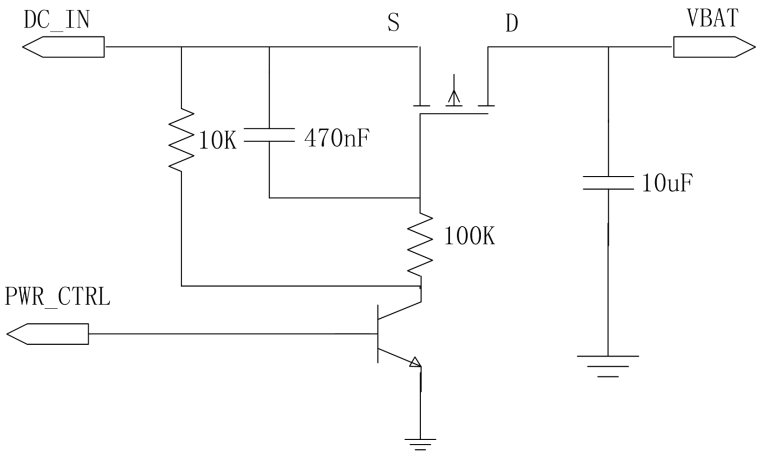

Figure 3-5 PMOS tube control power switch reference circuit

NOTE

- ✧ To prevent damage to the module from surges and overvoltages, it is recommended to connect a 5.1V/500mW Zener diode to the VBAT pin of the module.
- ✧ It is recommended to add 3 ceramic capacitors (33pF, 10pF, 100nF) to the power pin input and place them near the VBAT pin.
- ✧ The minimum operating voltage of the module is 3.3V. Since the data is transmitted or the call will generate more than 2A, the ripple voltage drop will occur on the power supply voltage. Therefore, the actual supply voltage must not be lower than 3.3V.
- ✧ Due to the large current consumption of the module power pins, it is recommended that the PCB traces be as short as possible. Minimize the equivalent impedance of the VBAT trace.

3.3.3 VDD_EXT Voltage output

The CLM920 AC3 module outputs 1.8V through VDD_EXT for internal digital circuitry. This voltage is the logic level voltage of the module. After normal power-on, the 17th pin will output 1.8V and the current load will be 50mA. The external master can read the voltage of VDD_EXT to determine if the module is powered on. VDD_EXT can also be used as an external power supply, such as a level shifting chip.

3.4 Switching machine reset mode

3.4.1 Module boot

The 21 pin of the CLM920 AC3 module is the boot pin. The module can be powered down by PWRKEY for at least 500ms. The user can check whether the module is powered on by querying the high and low levels of the VDD_EXT pin.

When the CLM920 AC3 module is powered on, pull the PWRKEY pin low for at least 1S and release it. The module will perform shutdown process shutdown (this function is under development).

Table 3-5 Switching machine pin definition

Pin	Name	I/O	High value	Description
21	PWRKEY	PI	VBAT-0.3V	Active low

3.4.2 Boot timing

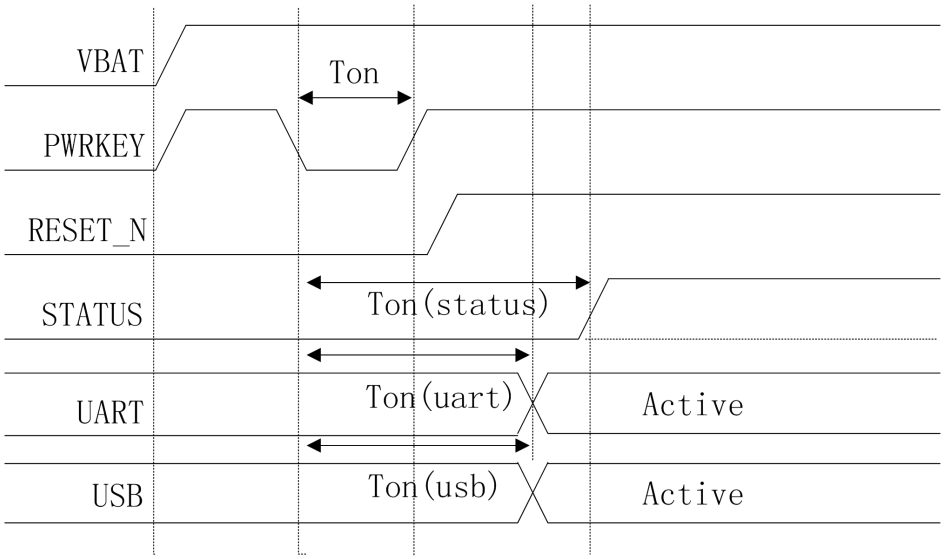

Figure 3-6 Startup timing diagram

Table 3-6 Boot timing parameters

Symbol	Description	Min	Typical	Max	unit
Ton	Boot low level width	100	500	-	ms
Ton(status)	Boot time (according to *status* status)	22	-	-	ms
Ton(usb)	Boot time (according to *usb* status)	-	10	-	s
Ton(uart)	Boot time (according to *uart* status)	-	6	-	s
VIH	PWRKEY Input high level	0.6	0.8	1.8	V
VIL	PWRKEY Input low level	-0.3	0	0.5	V

It is recommended to use the open-collector drive circuit to control the PWRKEY, which can be released after the base level is pulled for 500ms, and the module is powered on. Switching machine design can also be done with buttons, button accessories need to be placed with a TVS tube for ESD protection.

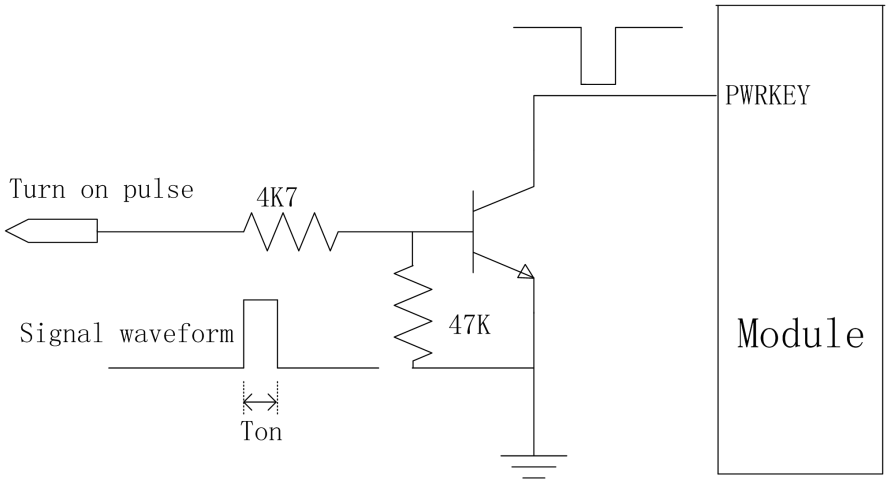

Figure 3-7 Open set drive start reference circuit

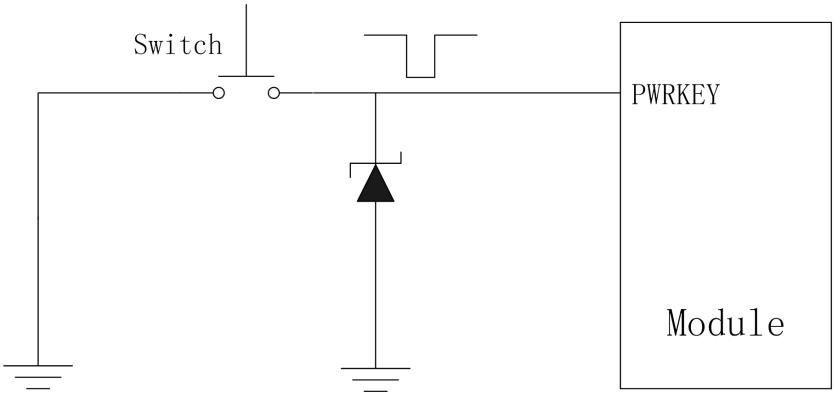

Figure 3-8 Button start reference circuit

3.4.3 Module shutdown

The CLM920 AC3 module supports the following three shutdown modes.

Table 3-7 Module shutdown mode

Shutdown mode	Shutdown condition	Description
Low voltage shutdown	The supply voltage is too low or abnormally powered down	The module did not perform a normal shutdown process
Hardware shutdown	Pull down the PWRKEY pin	Normal shutdown
AT command	AT command	Software shutdown

shutdown		

When the module is working normally, do not shut down the power by turning off the power, which may damage the module's Flash data. It is recommended to execute the shutdown process through the PWRKEY and AT commands.

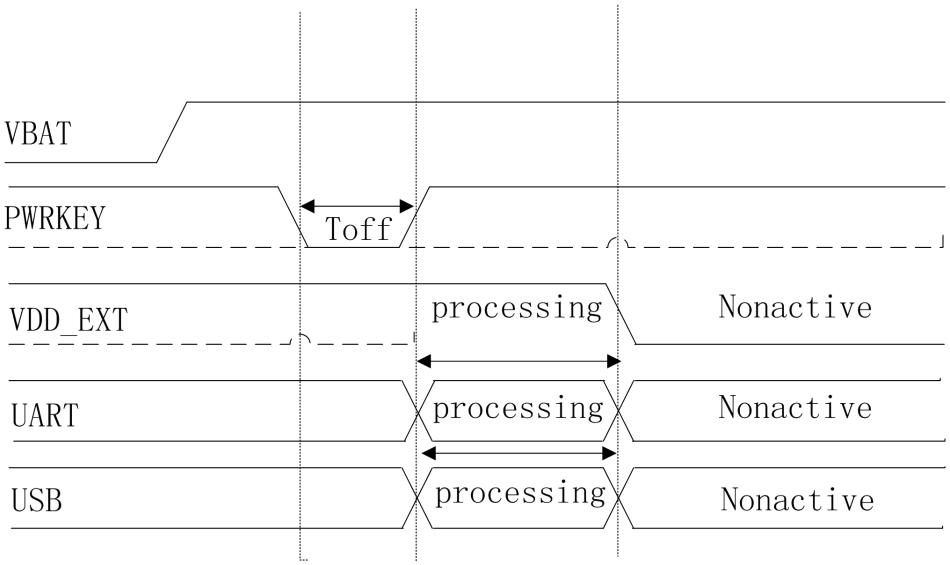

Figure 3-9 Shutdown timing diagram

3.4.4 Reset control

The CLM920 AC3 module PIN20 is a reset pin. The application detects that the module is abnormal. When the software does not respond, the module can be reset. Pull the pin low for 100-450ms to reset the module. The RESET pin is sensitive to interference. A 10nF to 0.1uF capacitor can be installed near the signal for signal filtering. Keep away from RF interference signals when routing.

Table 3-8 Reset foot definition

Pin	Signal name	I/O	High value	Description
20	RESET_N	PI	1.8V±0.3V	Active low

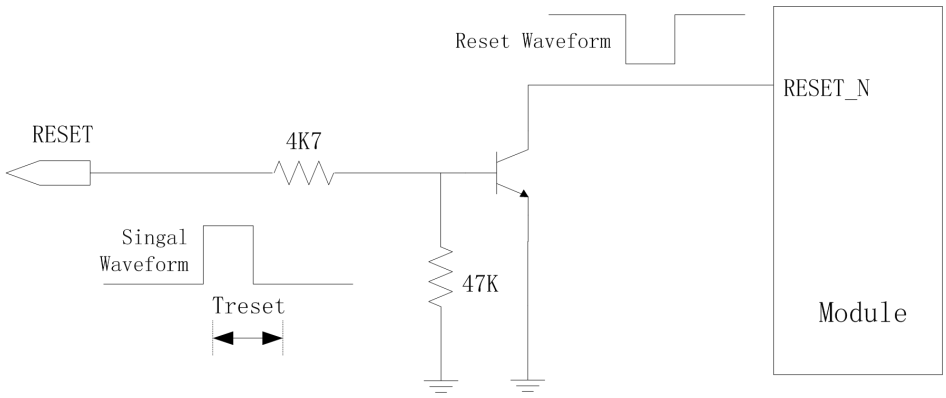

Figure 3-10 Reset Reference Circuit

Table 3-9 RESET pin parameters

Symbol	Description	Min	Typical	Max	unit
Treset	Low pulse width	150	200	450	ms
VIH	RESET input high level voltage	1.17	1.8	2.1	V
VIL	RESET input low level voltage	-0.3	0	0.8	V

Reset RESET timing is as follows：

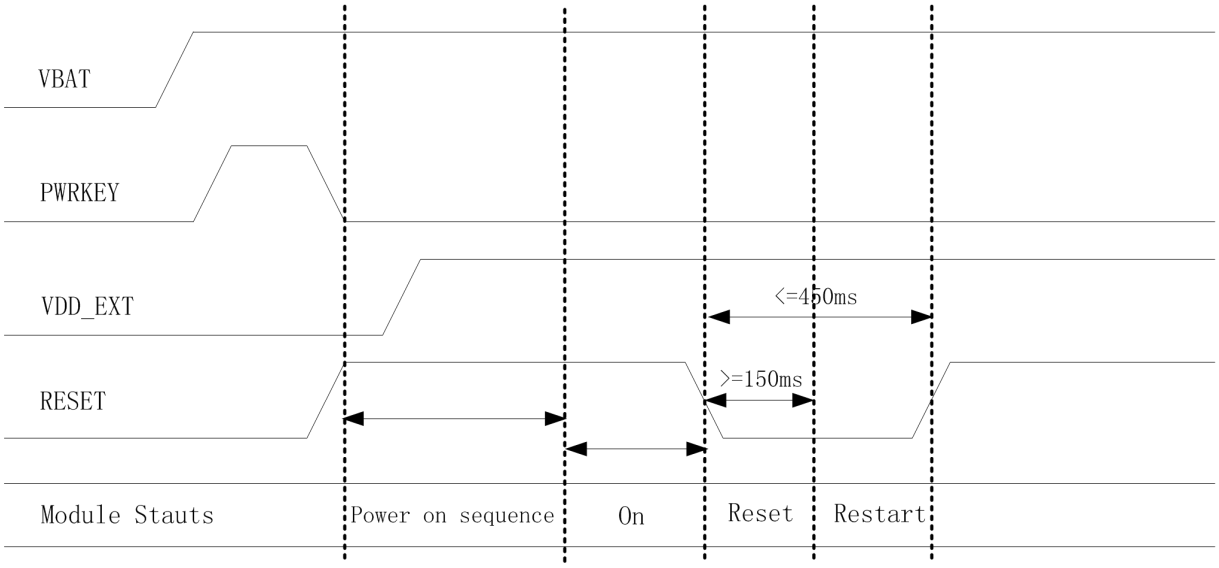

Figure 3-11 Reset timing diagram

The CLM920 AC3 module supports AT command reset, and the AT command is at+cfun=1,1 to restart the module. Detailed instructions can be found in the CLM920 AC3 AT Command Set Manual.

3.5 USB interface

The CLM920 AC3 module USB interface supports USB2.0 high-speed protocol, supports slave mode, and does not support USB charging mode. USB input and output traces must comply with the USB2.0 feature. The USB interface is defined as follows：

Table 3-10 USB interface pin definition

Pin number	Signal name	IO	Description
71	USB_VBUS	PI	USB insertion detection
70	USB_DM	IO	USB differential signal -
69	USB_DP	IO	USB differential signal +

The module acts as a USB slave device and supports USB sleep and wake-up mechanisms. USB interface application reference circuit is as follows：

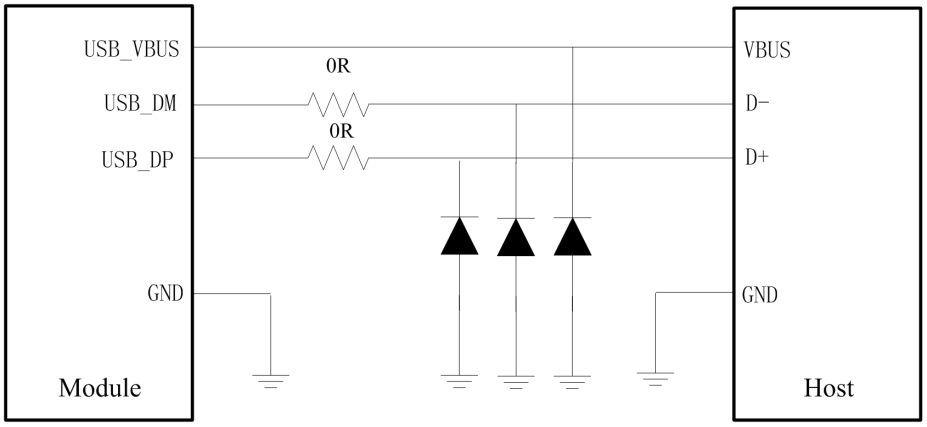

Figure 3-12 USB connection design circuit diagram

NOTE

- ✧ The USB interface supports high-speed (480Mbps) and full-speed (12Mbps) modes. Therefore, the trace design needs to strictly follow the USB2.0 protocol requirements. Pay attention to the protection of the data lines, differential traces, and control impedance of 90Ω.
- ✧ In order to improve the antistatic performance of the USB interface, it is recommended to add an ESD protection device on the data line. The equivalent capacitance of the protection device is less than 2pF. It is recommended to connect a 0 ohm resistor in series

with the data line.

- ✧ The USB interface of the module does not provide USB bus power, and the module can only be used as a slave device of the USB bus device.
- ✧ The USB interface can support functions such as software download upgrade, data communication, AT Command and other functions.。

3.6 UART interface

The CLM920 AC3 module provides two sets of UART interfaces. Main serial port and debug serial port, serial port level is 1.8V.

3.6.1 Main serial port

Main serial port：

The serial port can realize AT interactive instructions, print program log information, and interact with peripheral data.

The module's serial port baud rate can be set to 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600bps baud rate, the default is 115200bps.

The UART interface is defined as follows：

Table 3-11 Main serial port signal definition

Pin	name	I/O	Description	parameter	Level value (V)			Remarks
					Min	Typical	Max	
62	RI	DO	UART ringing output	VOH	1.35	1.8	2	
				VOL	0		0.45	
63	DCD	DO	UART data carrier detection	VOH	1.35	1.8	2	
				VOL	0		0.45	
64	CTS	DO	UART clear send	VOH	1.35	1.8	2	
				VOL	0		0.45	
65	RTS	DI	Send UART request	VIH	1.2	1.8	2	
				VIL	-0.3		0.6	
67	TXD	DO	UART send data	VOH	1.35	1.8	2	
				VOL	0		0.45	

68	RXD	DI	UART receive data	VIH	1.2	1.8	2	
				VIL	-0.3		0.6	

When the user wants to use the 4-wire serial port, you can refer to the following connection methods

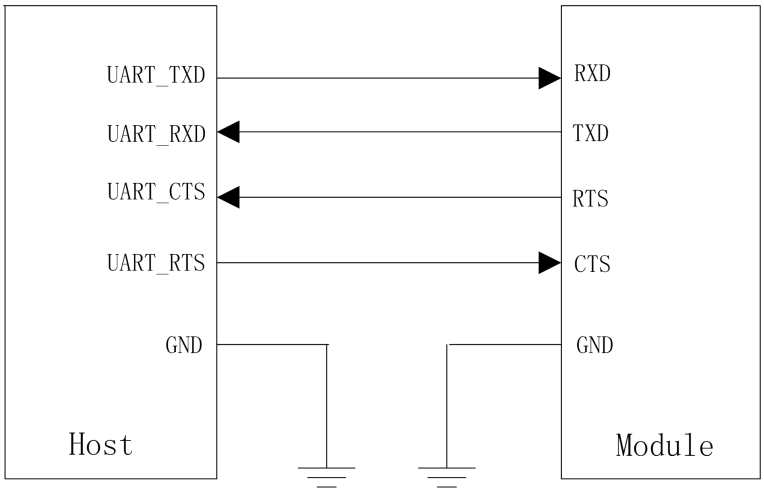

Figure 3-13 Four-wire serial port design

If you need to use a 2-wire serial port, you can refer to the following serial port design.

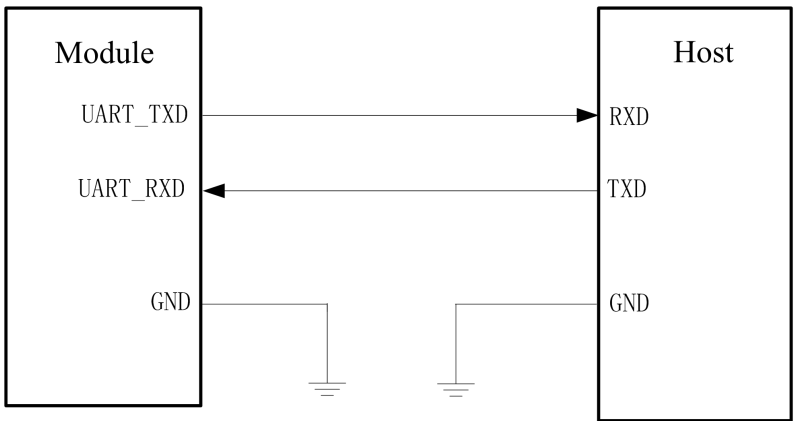

Figure 3-14 Two-wire serial port design

The serial port of the module is TTL 1.8V level. If the serial port needs to be connected with the MCU of 3.3V level, it needs to externally add a level conversion chip to achieve level matching. The chip connection method can refer to the following circuit:

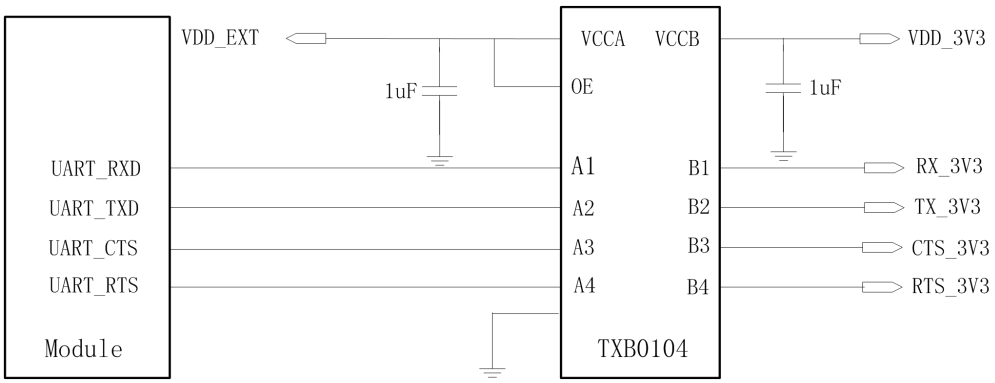

Figure 3-15 Level conversion chip circuit

3.6.2 Debug serial port

The 11th and 12th pins of the module are debug serial port pins, and the debug serial port supports 115200bps baud rate. It is used for Linux control and log printing. It can reserve test points for module debugging. Please do not leave it floating.

Table 3-12 Debugging serial port pin definitions

Pin	Signal name	I/O	Description	Parameter	Level value (V)			Remarks
					Min	Typical	Max	
11	DBG_RXD	DI	UART data reception	VIH	1.2	1.8	2	
				VIL	-0.3		0.6	
12	DBG_TXD	DO	UART data transmission	VOH	1.35	1.8	2	
				VOL	0		0.45	

3.6.3 RI Signal interface

The CLM920 AC3 module supports the serial sleep wake-up function, and the RI pin can be used as an interrupt to wake up the host.

RI:

The RI pin can wake up the host as an interrupt.

The RI pin idle state is low. When a short message or voice incoming call is received, the RI outputs a rectangular wave with a period of 500ms (high level for 250ms, low level for 250ms) to wake up the host.。

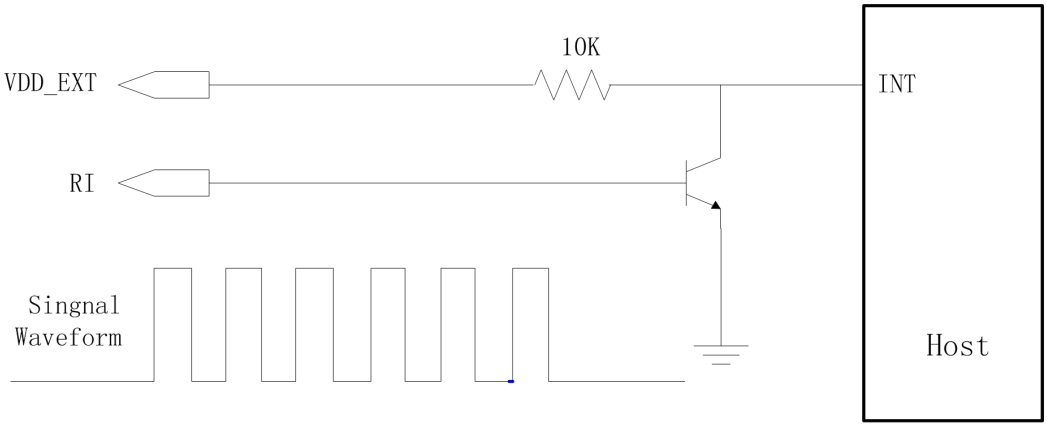

Figure 3-16 RI pin signal waveform

Send AT+DISABLEUSB=1, AT+CSCLK=1, after the module enters sleep.

3.7 USIM interface

The CLM920 AC3 module provides a USIM card interface compatible with the ISO 7816-3 standard. The USIM card power supply is provided by the module's internal power manager and supports 1.8V/3.0V voltage.

Table 3-13 SIM card signal definition

Pin	Name	I/O	Description	Parameter	Level value (V)			Remarks
					Min	Typical	Max	
13	USIM_PRESENCE	DI	USIM card detection	VIH	1.6	1.8	2	If you do not use hot plug power, leave it floating.
				VIL	0		0.18	
14	USIM_VDD	PO	USIM card power supply	V3.0	2.75	3.0	3.05	USIM_VDD= 3.0V
				V1.8	1.75	1.8	1.95	USIM_VDD= 1.8V
15	USIM_DATA	IO	USIM card data	VIH	0.65* VDD		3.05	USIM_VDD: 3.0V/1.8V
				VIL	-0.3	0	0.25* VDD	

				VOH	VDD-0.45		3.05	
				VOL	0	0	0.45	
16	USIM_CLK	DO	USIM card clock	VOH	VDD-0.45		3.05	USIM_VDD: 3.0V/1.8V
				VOL	0	0	0.45	
17	USIM_RST	DO	USIM card reset	VOH	VDD-0.45		3.05	USIM_VDD: 3.0V/1.8V
				VOL	0	0	0.45	

3.7.1 USIM card reference circuit

The CLM920 AC3 module does not come with a USIM card slot. Users need to design a USIM card slot on their own interface board. USIM card interface reference circuit is as follows：

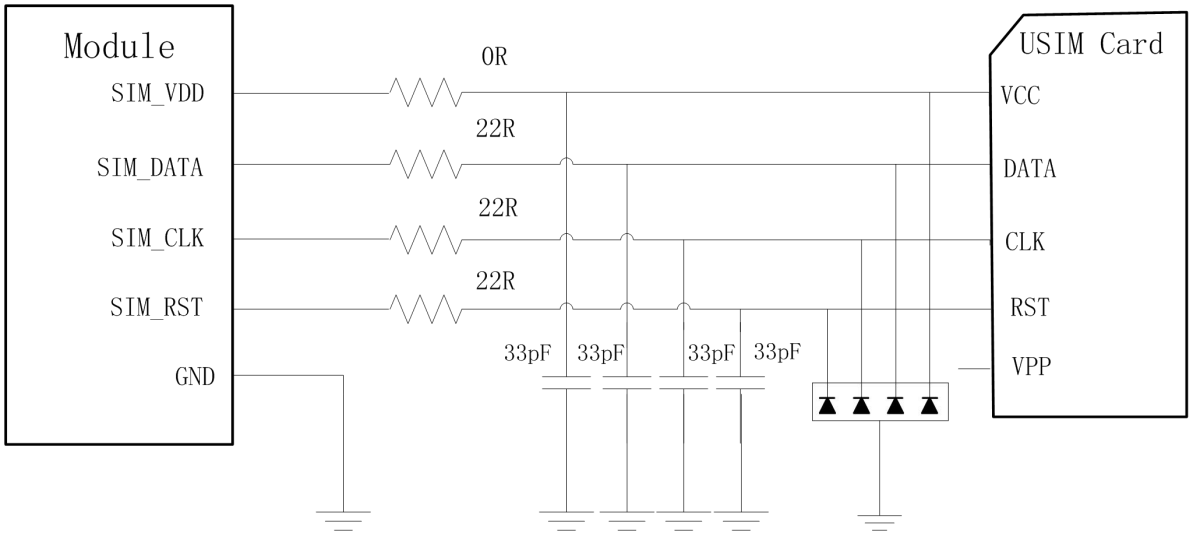

Figure 3-17 USIM design circuit diagram

NOTE

- ✧ The USIM interface cable is recommended to use ONSEMI's SMF15C device for ESD protection. The peripheral circuit components should be placed close to the card holder, and the SIM card holder is close to the module layout.
- ✧ The USIM card circuit is susceptible to radio frequency interference and does not recognize or drop the card. Therefore, the card slot should be placed as far as possible

from the RF radiation of the antenna. The card trace should be as far away as possible from the RF, power supply and high-speed signal lines.

- ✧ There is no pull-up resistor inside USIM_DATA, which requires an external 47K resistor to be pulled up to VDD_EXT.
- ✧ USIM_PRESENCE inserts or inserts the detection pin for the USIM card. It is high by default. The SIM card status can be detected by this PIN pin during hot plug application.
- ✧ To avoid transient voltage overload, the USIM interface requires a 22R resistor in series with each other on the signal line path.
- ✧ The ground of the USIM deck and the ground of the module should maintain good connectivity.

3.7.2 USIM_ PRESENCE Hot Swap Reference Design

The CLM920 AC3 module supports the hot plugging function of the USIM card. The USIM_PRESENCE pin acts as an input detection pin to determine whether the USIM card is inserted or not. The USIM_PRESENCE pin defaults to a pull-up high. The hot plug function can be turned on or off by AT+HOSCFG. This function is off by default (see the CLM920 AC3 AT command set for details)。

Table 3-14 SIM card hot swap detection pin definition

NO.	AT command	USIM_PRESENCE status	Functional description
1	AT+HOSCFG=1,1	high	SIM card insertion, detection foot is high
2	AT+HOSCFG=1,0	low	SIM card insertion, detection pin is low

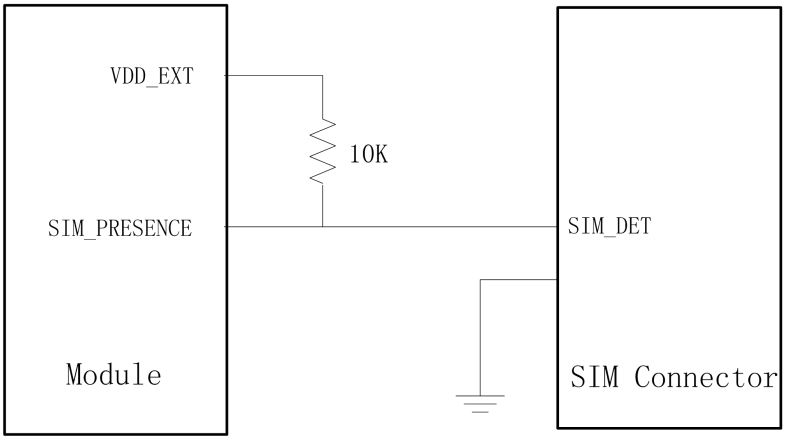

Figure 3-18 Hot swap detection of the USIM card

NOTE

- ✧ It is recommended to add a diode protection next to the USIM_PRESENCE pin of the module.
- ✧ When using a normally closed SIM card holder or a normally open SIM card holder, the detection function can be set by the AT command. If AT+HOSCFG=1 is set, the status of the SIM card is high when the SIM card is in place, and AT+HOSCFG=1 is set. When the SIM card is in the state, the status is low. Set AT+HOSCFG=0.0 SIM card hot swap function is off.

3.8 General purpose GPIO interface

The CLM920 AC3 module contains three general control signals. The interface is defined as follows：

Table 3-15 General GPIO Pin Definitions

Pin	Signal name	I/O	Description	Para meter	Level value (V)			Remarks
					Min	Typical	Max	
1	WAKEUP_IN	DI	Sleep mode control	VIH	1.2	1.8	2	
				VIL	-0.3		0.6	
2	AP_READY	DI	Sleep state detection	VIH	1.2	1.8	2	Developing
				VIL	-0.3		0.6	
4	W_DISABLE#	DI	Flight mode control	VIH	1.2	1.8	2	Developing
				VIL	-0.3		0.6	

WAKEUP_IN:

This pin is the host wake-up module pin. When the WAKEUP_IN signal is pulled low, the host can wake up the module.

AP_READY(This feature is under development)

AP_READY This pin can be used to wake up the host from the module and can be configured to wake up high or low.。

W_DISABLE#:

Flight mode control (this function is under development), when the CLM920 AC3 module W_DISABLE# signal is pulled low, the module RF function can be turned off, the module can enter the flight mode, and the module can be turned on to open the module RF function.

It can also be set to flight mode by AT+CFUN. For details, please refer to CLM920 AC3 AT command set.

3.9 Status indication interface

The CLM920 AC3 module provides three GPIO pins to indicate module status.

Table 3-16 Network indication pin definition

Pin	Name	I/O	Description
5	NET_MODE	DO	4G network indication, function developing
6	NET_STATUS	DO	Network indication
61	STATUS	DO	Module status indication

Table 3-17 Network operation status indication

status	LED display status
Module registration failed	Constantly bright
Module registration 4G or registration 3G for data service	Flashing

Table 3-18 Module status indication

Module power on status indication	Pin level
Boot	low
其他	High resistance

The module network indicator reference design is as follows:

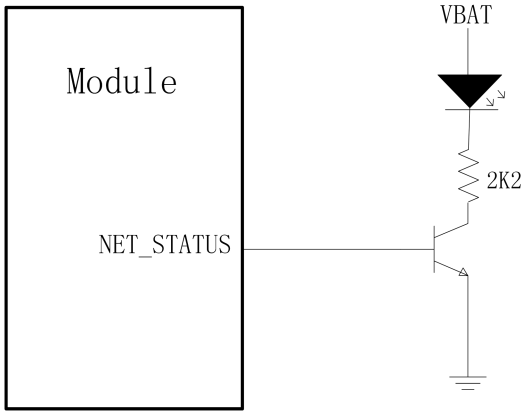

Figure 3-19 Network indicator circuit diagram

NOTE

The brightness of the network indicator can be adjusted by adjusting the current limiting resistor R. The current can be adjusted up to 40mA.。

3.10 PCM digital voice interface (under developing)

The CLM920 AC3 module provides a set of PCM digital audio interfaces for communication with external CODE audio devices. The set of PCM supports 8-bit A rate, U rate and 16-bit linear short frame coding format. Interface signal PCM_SYNC is 8kHZ, PCM_CLK is 2048kHZ。

Table 3-19 PCM pin definition

Pin	Name	I/O	Description	para meter	Level value (V)			Remarks
					Min	Typical	Max	
24	PCM_IN	DI	PCM data input	VIH	1.2	1.8	2	
				VIL	-0.3		0.6	
25	PCM_OUT	DO	PCM data output	VOH	1.35	1.8	2	
				VOL	0		0.45	
26	PCM_SYNC	DO	PCM frame sync signal	VOH	1.35	1.8	2	
				VOL	0		0.45	
27	PCM_CLK	DO	PCM clock pulse	VOH	1.35	1.8	2	
				VOL	0		0.45	

Table 3-20 PCM specific parameters

Characteristic	Description
Encoding format	Linear
Data bit	16bits
Master-slave mode	Master/slave mode
PCM clock	2048kHz
PCM frame synchronization	Short frame
Data Format	MSB

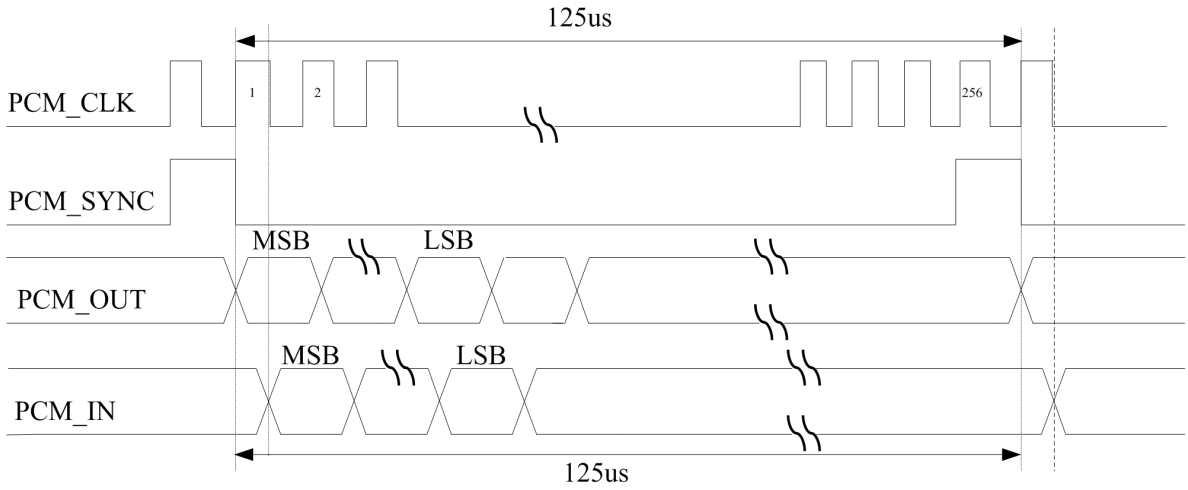

Figure 3-20 PCM short frame mode timing diagram

PCM to analog voice recommendation circuit is as follows：

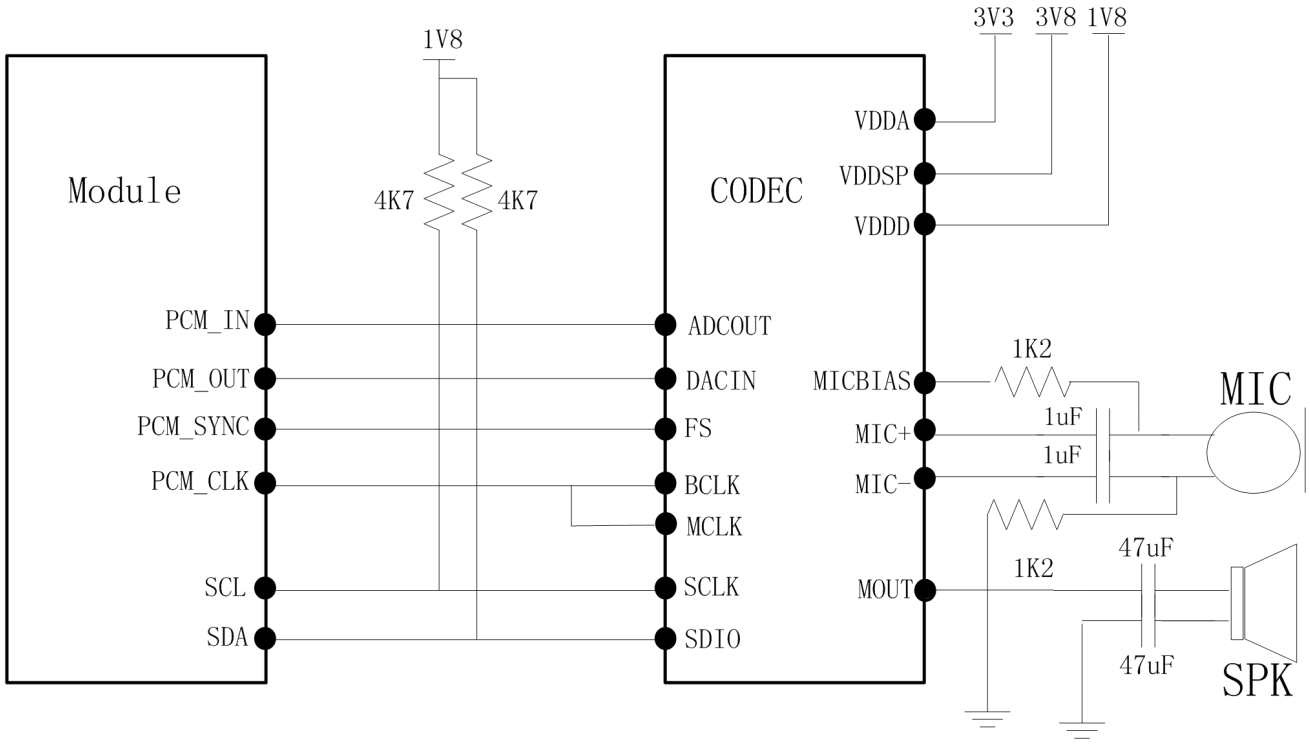

Figure 3-21 PCM to analog voice map

3.11 I2C bus (under developing)

The CLM920 AC3 module provides a set of hardware bidirectional serial buses with an I2C interface of 1.8V level, a 5.0 protocol interface, and a clock rate of 400KHz.

Table 3-21 I2C pin definition

Pin	Name	I/O	Description	Parameter	Level value (V)			Remarks
					Min	Typical	Max	
41	I2C_SCL	DO	I2C bus clock output	VOH	1.35	1.8	2	
				VOL	0		0.45	
42	I2C_SDA	IO	I2C bus data input and output	VOH	1.35	1.8	2	
				VOL	0		0.45	
				VIH	1.2	1.8	2	
				VIL	-0.3		0.6	

I2C reference circuit connection is as follows：

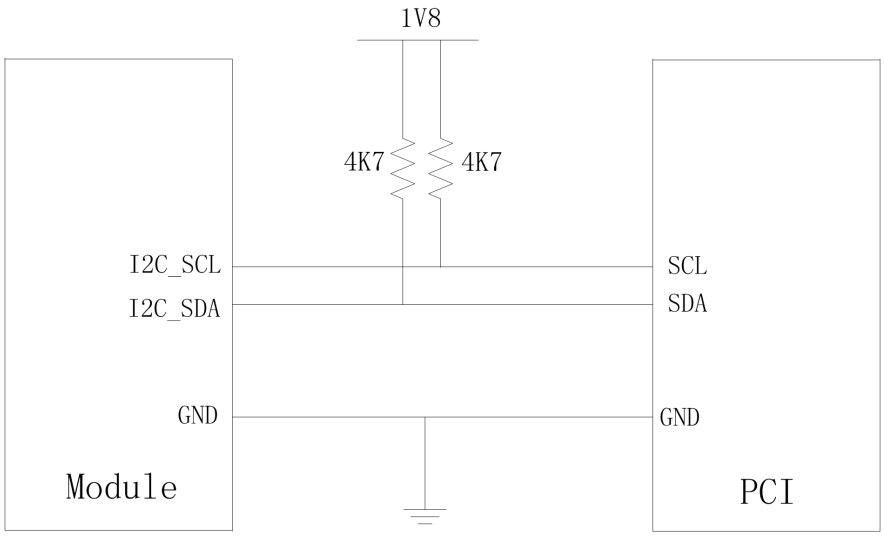

Figure 3-22 I2C interface reference circuit diagram

3.12 WLAN interface (under developing)

The CLM920 AC3 module provides a SDIO interface that supports the SD3.0 protocol for WLAN wireless connections. Currently WLAN function developing。

Table 3-22 Wireless connection pin definition

Pin	Name	I/O	Description
28	WLAN_WAKE_HOST	DO	WLAN wake up HOST
29	WLAN_CLK	DO	WLAN SDIO clock
30	WLAN_CMD	IO	WLAN SDIO command
31	SDC_DATA0	IO	WLAN SDIO bus DATA0
32	SDC_DATA1	IO	WLAN SDIO bus DATA1
33	SDC_DATA2	IO	WLAN SDIO bus DATA2
34	SDC_DATA3	IO	WLAN SDIO bus DATA3
37	WLAN_CLK_EN	DO	External clock enable control pin
38	WLAN_CLK_26M	DO	26MHZ clock
39	WLAN_PDN	DO	Power saving mode control
40	WLAN_DC_EN	DO	DCDC enable control pin

NOTE

The SDIO bus speed is fast, and the Layout trace must conform to the SDIO3.0 specification.

- ✧ The length of the signal line should be less than 50mm, the spacing of the signal line should be 2 times the line width and cover the ground and be as far away as possible from other possible interference lines;
- ✧ The WLAN_CLK signal line is connected in series with a matching resistor on the module end, and the trace needs to be processed in the package.。

3.13 ADC interface

The CLM920 AC3 provides two analog-to-digital converter interfaces to read the voltage value. The input voltage of the ADC interface cannot exceed 1.3V. It is recommended that the ADC pin be input with a voltage divider circuit.

Table 3-23 ADC Pin Definitions

Pin	Name	Description	Level value (V)			Remarks
			Min	Typical	Max	
44	ADC1	Analog to digital	0.3		1.3V	ADC

		converter interface 1				resolution12bits
45	ADC0	Analog to digital converter interface 0	0.3		1.3V	ADC resolution 12bits

3.14 RF interface

The CLM920 AC3 module provides two antenna interfaces, one main set antenna interface, which is responsible for the 4G and 3G signals of the transceiver module, and one diversity antenna interface. It is responsible for receiving 4G and 3G signals. The signal degradation caused by multi-path and high-speed movement can be passed. Adding a diversity antenna enhances the signal. The impedance of the two antenna interfaces is 50 ohms. 4G recommends connecting diversity antennas to limit high-speed movement and signal degradation caused by multipath.

Table 3-24 Antenna interface pin definition

Pin	Name	I/O	Description	Remarks
49	ANT_MAIN	IO	Main antenna interface	50 ohm characteristic impedance
35	ANT_DIV	AI	Diversity antenna interface	50 ohm characteristic impedance

3.14.1 Antenna matching circuit

The 49-pin of the CLM920 AC3 is the main set antenna interface. To facilitate the debugging of the antenna, a π-type matching circuit needs to be added to the main board, and the 50-ohm impedance line is taken.

The 35-pin of the CLM920 AC3 is a diversity antenna interface. To facilitate antenna debugging, a π-type matching circuit needs to be added to the motherboard, and a 50-ohm impedance line is taken.

Recommended circuit as shown below：

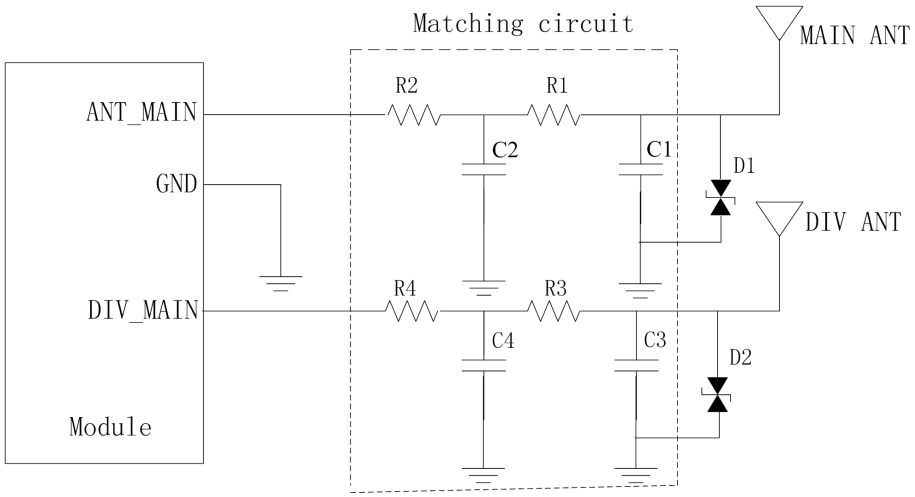

Figure 3-23 Antenna matching circuit

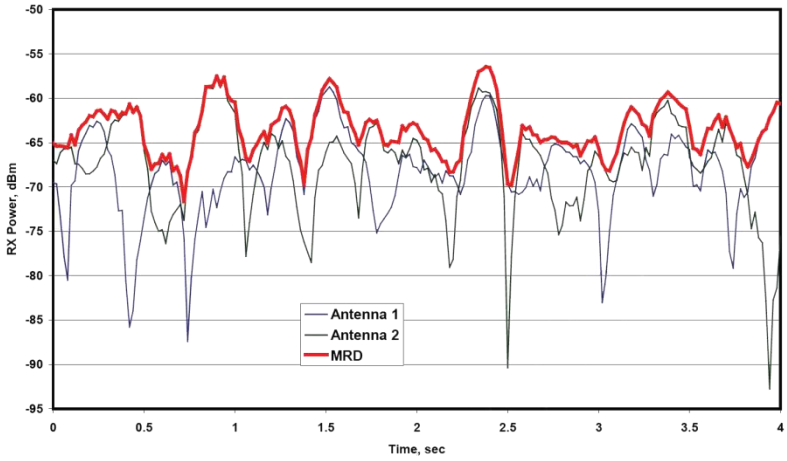

Figure 3-24 Comparison of received signal strengths with and without diversity antennas

NOTE

- ✧ The CLM920 AC3 module provides two RF antenna interfaces, which are the main set antenna and the diversity antenna respectively. The antenna interface must be a 50 ohm characteristic impedance trace.
- ✧ The main antenna and the diversity antenna are distributed reasonably to improve the receiving sensitivity.
- ✧ In actual use, the antenna board can be debugged and optimized according to the user's circuit board. The motherboard R1/R2/R3/R4 defaults to 33pF, and C1/C2/C3/C4 defaults to empty. During this period, it is recommended to attach a bidirectional TVS

tube at the D1/D2 of the antenna connection.

- ✧ The parasitic capacitance of the TVS tube pins themselves must be small to avoid signal interference. The ESD protection component used on the antenna must take into account the frequency band used by the antenna and the minimum parasitic capacitance that can be accepted by different frequency bands. The ESD protection component usually used on the antenna must have a parasitic capacitance value of less than 0.5pF or even more. low.
- ✧ Antenna impedance traces need to be away from digital signal lines, power supplies and other interference signals.
- ✧ The antenna impedance traces need to be three-dimensionally packaged, and the ground holes are added on both sides of the trace to isolate.

3.14.2 RF trace reference

The main set and diversity antenna of the CLM920 AC3 module are extracted by pad. The antenna pad to the antenna feed point must use microstrip lines or other types of RF traces. The characteristic impedance of the signal line should be controlled at 50Ω.

The impedance of the RF RF signal line is determined by the material's dielectric constant, trace width (W), ground clearance (S), and reference ground plane height (H). Therefore, the RF trace requires an impedance simulation tool to calculate the impedance of the RF trace.

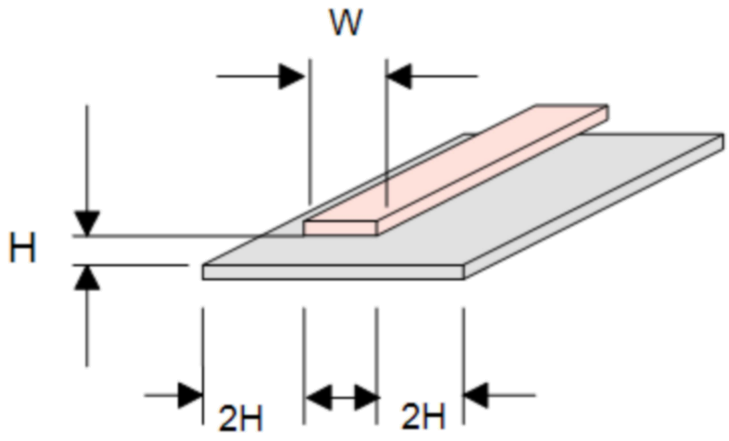

Figure 3-25 Complete structure of the microstrip line

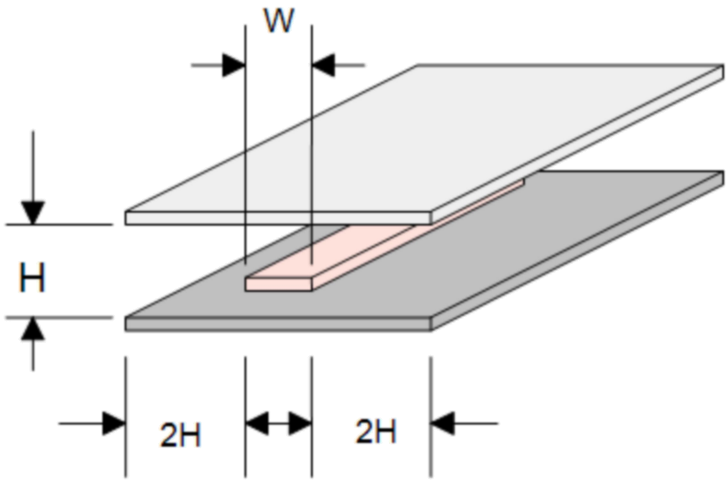

Figure 3-26 Complete structure of the strip line

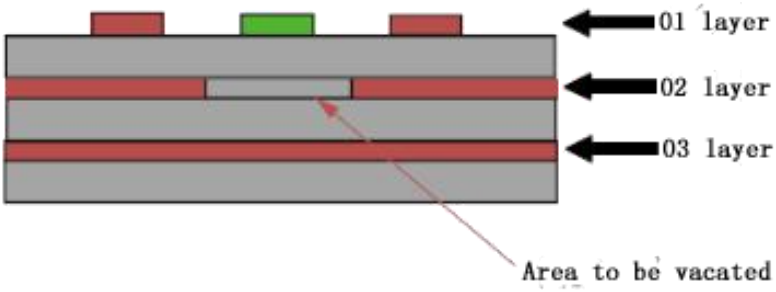

Figure 3-27 Reference ground is the third layer PCB microstrip transmission line structure

Chapter 4. Overall Technical Indicators

4.1 Chapter overview

The CLM920 AC3 module RF overall specifications include the following sections:

- ✧ Working frequency;
- ✧ Conducted radio frequency measurement;
- ✧ Conducted receiving sensitivity and transmitting power;
- ✧ Antenna requirements
- ✧ Module power consumption characteristics

4.2 Working frequency

Table 4-1 RF frequency table

Frequency band	Uplink frequency	Downstream frequency	Duplex mode
LTE B1	1920MHz－1980MHz	2110MHz－2170MHz	FDD
LTE B3	1710MHz－1785MHz	1805MHz－1880MHz	FDD
LTE B5	824MHz－849MHz	869MHz－894MHz	FDD
LTE B8	880MHz－915MHz	925MHz－960MHz	FDD
LTE B34	2010MHz－2025MHz	2010MHz－2025MHz	TDD
LTE B38	2570MHz－2620MHz	2570MHz－2620MHz	TDD
LTE B39	1880MHz－1920MHz	1880MHz－1920MHz	TDD
LTE B40	2300MHz－2400MHz	2300MHz－2400MHz	TDD
LTE B41	2555MHz－2655MHz	2555MHz－2655MHz	TDD
UMTS B1	1920MHz－1980MHz	2110MHz－2170MHz	WCDMA
UMTS B5	824MHz－849MHz	869MHz－894MHz	WCDMA
UMTS B8	880MHz－915MHz	925MHz－960MHz	WCDMA

4.3 Conducted radio frequency measurement

4.3.1 Test environment

Table 4-2 Test instruments

Test instrument	Power supply	Murata coaxial RF line

R&S CMW500	Agilent 66319	MXHP32HP1000

4.3.2 Standard test

The CLM920 AC3 module passes the 3GPP TS 51.010-1, 3GPP TS 34.121-1, 3GPP TS 36.521-1, 3GPP2 C.S0011 and 3GPP2 C.S0033 test standards. Each module passes rigorous testing at the factory to ensure reliable quality.

4.4 Conducted receiving sensitivity and transmit power

CLM920 AC3 module 3G receiving sensitivity and transmit power test indicators are as follows：

Table 4-3 3G RF Specifications

mode	Upstream	Down	power	Receiving sensitivity
WCDMA B1	1920MHz–1980MHz	2110MHz–2170MHz	23+2/-2dBm	<-109dBm
WCDMA B5	824MHz–849MHz	869MHz–894MH	23+2/-2dBm	<-109dBm
WCDMA B8	880MHz–915MHz	925MHz–960MHz	23+2/-2dBm	<-109dBm

CLM920 AC3 module 4G receiving sensitivity and transmit power test indicators are as follows：

Table 4-4 4G RF sensitivity indicators

Directory (sensitivity) (sensitivity)	3GPP protocol requirements	min	typical	max
LTE B1(FDD QPSK pass>95%)	< - 96.3(10MHz)		-101	-100
LTE B3(FDD QPSK pass>95%)	< - 93.3(10MHz)		-99.7	-99
LTE B5(FDD QPSK pass>95%)	< - 94.3(10MHz)		-102.7	-101
LTE B8(TDD QPSK pass>95%)	< - 93.3(10MHz)		-102.7	-101
LTE B34(TDD QPSK pass>95%)	< - 93.3(10MHz)		-97.2	-96
LTE B38(TDD QPSK pass>95%)	< - 96.3(10MHz)		-99.2	-98

LTE B39(TDD QPSK pass>95%)	< - 96.3(10MHz)		-99.2	-98
LTE B40(TDD QPSK pass>95%)	< - 96.3(10MHz)		-100.2	-99
LTE B41(TDD QPSK pass>95%)	< - 94.3(10MHz)		-98.7	-97

Table 4-5 4G RF transmit power specifications

Directory	3GPP Protocol Requirements (dBm)	min	typical	max
LTE B1	21 to 25	22	23	24
LTE B3	21 to 25	22	23	24
LTE B5	21 to 25	22	23	24
LTE B8	21 to 25	22	23	24
LTE B34	21 to 25	22	23	24
LTE B38	21 to 25	22	23	24
LTE B39	21 to 25	22	23	24
LTE B40	21 to 25	22	23	24
LTE B41	21 to 25	22	23	24

4.5 Antenna requirements

CLM920 AC3 Module Antenna Design Requirements:

Table 4-6 Antenna indicator requirements

Frequency band	Standing wave ratio	Gain	effectiveness	TRP	TIS
B1 FDD	<2.5:1	≤2.5dbi	>40%	>16.5	<-88
B3 FDD	<2.5:1	≤2.5dbi	>40%	>16.5	<-88
B5 FDD	<2.5:1	≤2.5dbi	>40%	>16.5	<-88
B8 FDD	<2.5:1	≤2.5dbi	>40%	>16.5	<-88
B34 FDD	<2.5:1	≤2.5dbi	>40%	>16.5	<-88
B38 TDD	<2.5:1	≤2.5dbi	>40%	>16.5	<-88
B39 TDD	<2.5:1	≤2.5dbi	>40%	>16.5	<-88
B40 TDD	<2.5:1	≤2.5dbi	>40%	>16.5	<-88
B41 TDD	<2.5:1	≤2.5dbi	>40%	>16.5	<-88
WB1	<2.5:1	≤2.5dbi	>40%	>18	<-105
W B5	<2.5:1	≤2.5dbi	>40%	>18	<-105

WB8	<2.5:1	≤2.5dbi	>40%	>18	<-105

4.6 Power consumption characteristics

Table 4-7 Sleep and idle power consumption of the three major operators

Operator	System	condition	mode	Current consumption mA
CTCC	LTE	Without USB connection	Sleep mode	Reserved
			Idle mode	Reserved
CMCC	LTE	Without USB connection	Sleep mode	Reserved
			Idle mode	Reserved
CUCC	WCDMA	Without USB connection	Sleep mode	Reserved
			Idle mode	Reserved
	LTE	Without USB connection	Sleep mode	Reserved
			Idle mode	Reserved

Table 4-8 WCDMA call power consumption

Frequency band	Power level	Current consumption mA
WCDMA B1	23dBm	Reserved
WCDMA B5	23dBm	Reserved
WCDMA B8	23dBm	Reserved

Table 4-9 HSDPA data transmission power consumption

Frequency band	Power dBm	Current consumption mA
WCDMA B1	23	Reserved
WCDMA B5	23	Reserved
WCDMA B8	23	Reserved

Table 4-10 LTE data transmission power consumption

Frequency band	Test bandwidth	Current consumption mA
LTE-FDD B1	@5Mbps	Reserved
	@10Mbps	Reserved
	@20Mbps	Reserved
LTE-FDD B3	@5Mbps	Reserved

	@10Mbps	Reserved
	@20Mbps	Reserved
LTE-FDD B5	@5Mbps	Reserved
	@10Mbps	Reserved
LTE-FDD B8	@5Mbps	Reserved
	@10Mbps	Reserved
LTE-FDD B34	@5Mbps	Reserved
	@10Mbps	Reserved
	@20Mbps	Reserved
LTE-TDD B38	@5Mbps	Reserved
	@10Mbps	Reserved
	@20Mbps	Reserved
LTE-TDD B39	@5Mbps	Reserved
	@10Mbps	Reserved
	@20Mbps	Reserved
LTE-TDD B40	@5Mbps	Reserved
	@10Mbps	Reserved
	@20Mbps	Reserved
LTE-TDD B41	@5Mbps	Reserved
	@10Mbps	Reserved
	@20Mbps	Reserved

Chapter 5. Interface Electrical Characteristics

5.1 Chapter overview

- ✧ Working storage temperature
- ✧ Module IO level
- ✧ Voltage
- ✧ Electrostatic property
- ✧ Reliability index

5.2 Working storage temperature

Table 5-1 CLM920 AC3 module working storage temperature

Parameter	Min	Max
Normal operating temperature	-30° C	75° C
Extreme working temperature	-40° C	85° C
Storage temperature	-40° C	85° C

5.3 Module IO level

CLM920 AC3 module IO level is as follows：

Table 5-2 Electrical Characteristics of CLM920 AC3 Module

Parameter	Parameter Description	Minimum	Maximum
VIH	High level input voltage	0.65* VDD_EXT	VDD_EXT+0.3V
VIL	Low level input voltage	-	0.35*VDD_EXT
VOH	High level output voltage	VDD_EXT-0.45V	VDD_EXT
VOL	Low level output voltage	0	0.45V

5.4 Voltage

CLM920 AC3 module input power requirements are as follows：

Table 5-3 Working voltage of CLM920 AC3 module

Parameter	Minimum	Typical	Maximum
Input voltage	3.3V	3.7V	4.2V

The power-on time of any interface of the module must not be earlier than the boot time of the module, otherwise the module may be abnormal or damaged.

5.5 Electrostatic property

There is no overvoltage protection inside the CLM920 AC3 module. The ESD protection is required when the module is used to ensure product quality.

ESD design recommendations:

- ✧ The USB port needs to add TVS on VDD, D+, D- for protection, and the TVS parasitic capacitance on D+/D- is <2pF;
- ✧ The module's USIM card external pin needs to be protected by TVS, and the parasitic capacitance requirement is <10pF.
- ✧ The PCB layout of the protective device should be as close as possible to the "V" line to avoid the "T" line.
- ✧ The ground plane around the module guarantees integrity and should not be split.
- ✧ ESD control of the surrounding environment and operators is required during module production, assembly and laboratory testing。

Table 5-4 CLM920 AC3 ESD Features

Test port	Contact discharge	Air discharge	unit
USB interface	±4	±8	KV
USIM interface	±4	±8	KV
VBAT power supply	±4	±8	KV

5.6 Reliability index

Table 5-5 CLM920 AC3 Reliability Test

Test items	Test Conditions	Guideline	Test Results
Low temperature work	Temperature: －40oC Working mode: normal work Test duration: 24h	IEC60068-2-1	Visual inspection: normal Function check: normal RF indicator check: normal
High	Temperature: 85oC	JESD2	Visual inspection: normal

temperature work	Working mode: normal work Test duration: 24h	2-A108-C	Function check: normal RF indicator check: normal
Temperature cycle	High temperature: 85oC Low temperature: －40oC Working mode: normal work Test duration: 30 Cycles;1h+1h/cycle	JESD22-A105-B	Visual inspection: normal Function check: normal RF indicator check: normal
Alternating hot and humid	High temperature: 55oC Low temperature: 25oC Humidity: 95% ± 3% Working mode: normal work Test duration: 6 Cycles;12h+12h/cycle	JESD22-A101-B	Visual inspection: normal Function check: normal RF indicator check: normal
Temperature shock	High temperature: 85oC Low temperature: －40oC Temperature change time: <30s Working mode: no packaging, no Power on, do not boot Test duration: 100 Cycles;15min+15min/cycle	JESD22-A106-B	Visual inspection: normal Function check: normal RF indicator check: normal
Drop test	Height 0.8m, 6 sides each time, dropped to the horizontal marble platform Working mode: no packaging, no Power on, do not boot	IEC60068-2-32	Visual inspection: normal Function check: normal RF indicator check: normal
Low temperature storage	Temperature: －40oC Working mode: no packaging, no power, no boot Test duration: 24 h	JESD22-A119-C	Visual inspection: normal Function check: normal RF indicator check: normal

High temperature storage	Temperature: 85oC Working mode: no packaging, no power, no boot Test duration: 24h	JESD22-A103-C	Visual inspection: normal Function check: normal RF indicator check: normal

Chapter 6.Structural and mechanical properties

6.1 Chapter overview

- ✧ Exterior
- ✧ Module mechanical size
- ✧

6.2 Exterior

The CLM920 AC3 module is a PCBA with a single-sided layout. The appearance of the module is as follows：

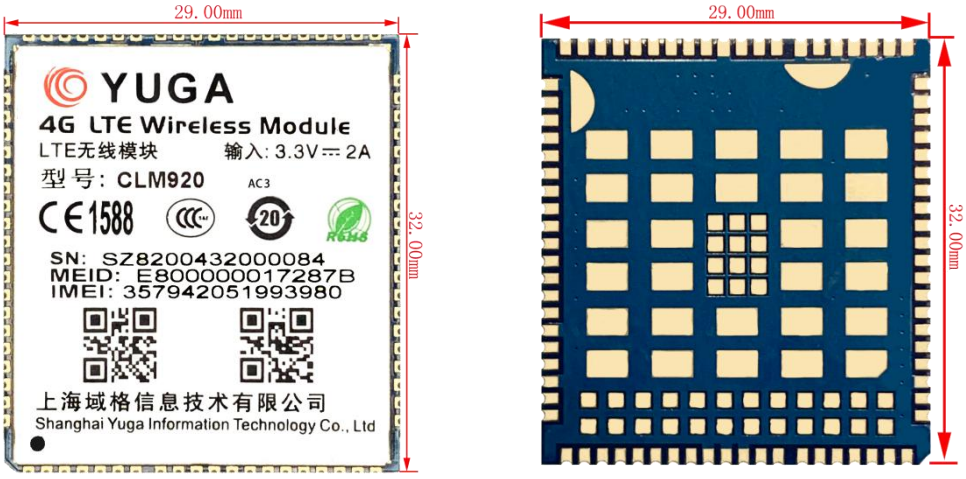

Figure 6-1 Appearance of the CLM920 AC3

6.3 Mechanical Dimensions

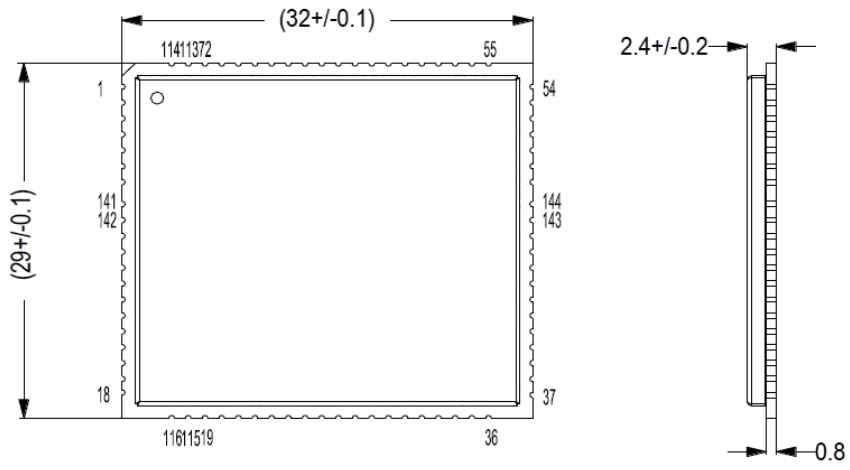

Figure 6-2 Front view and side view of the module (unit: mm)

The figure below shows the bottom view size of the module:

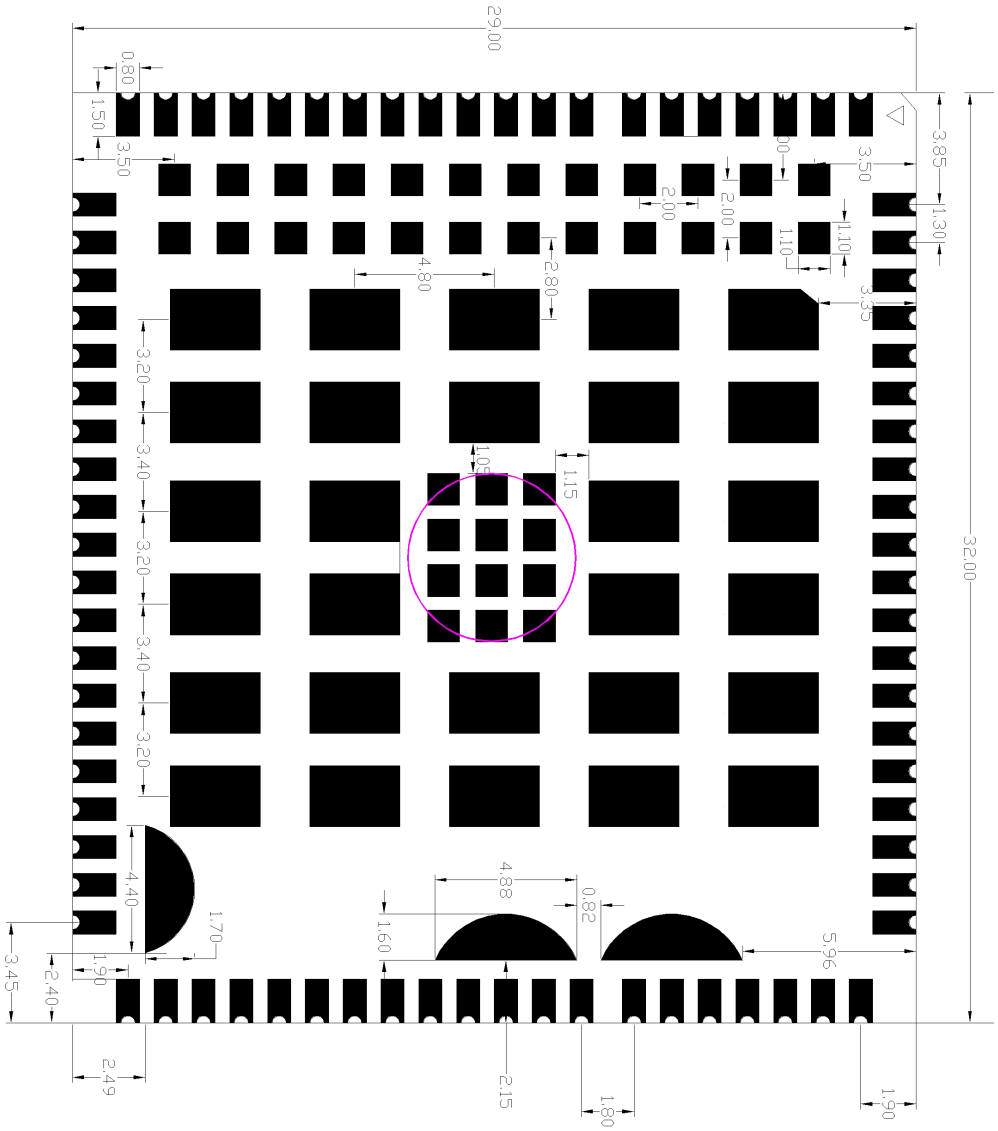

Figure 6-3 Bottom view of the module (unit: mm)

Module recommended package:

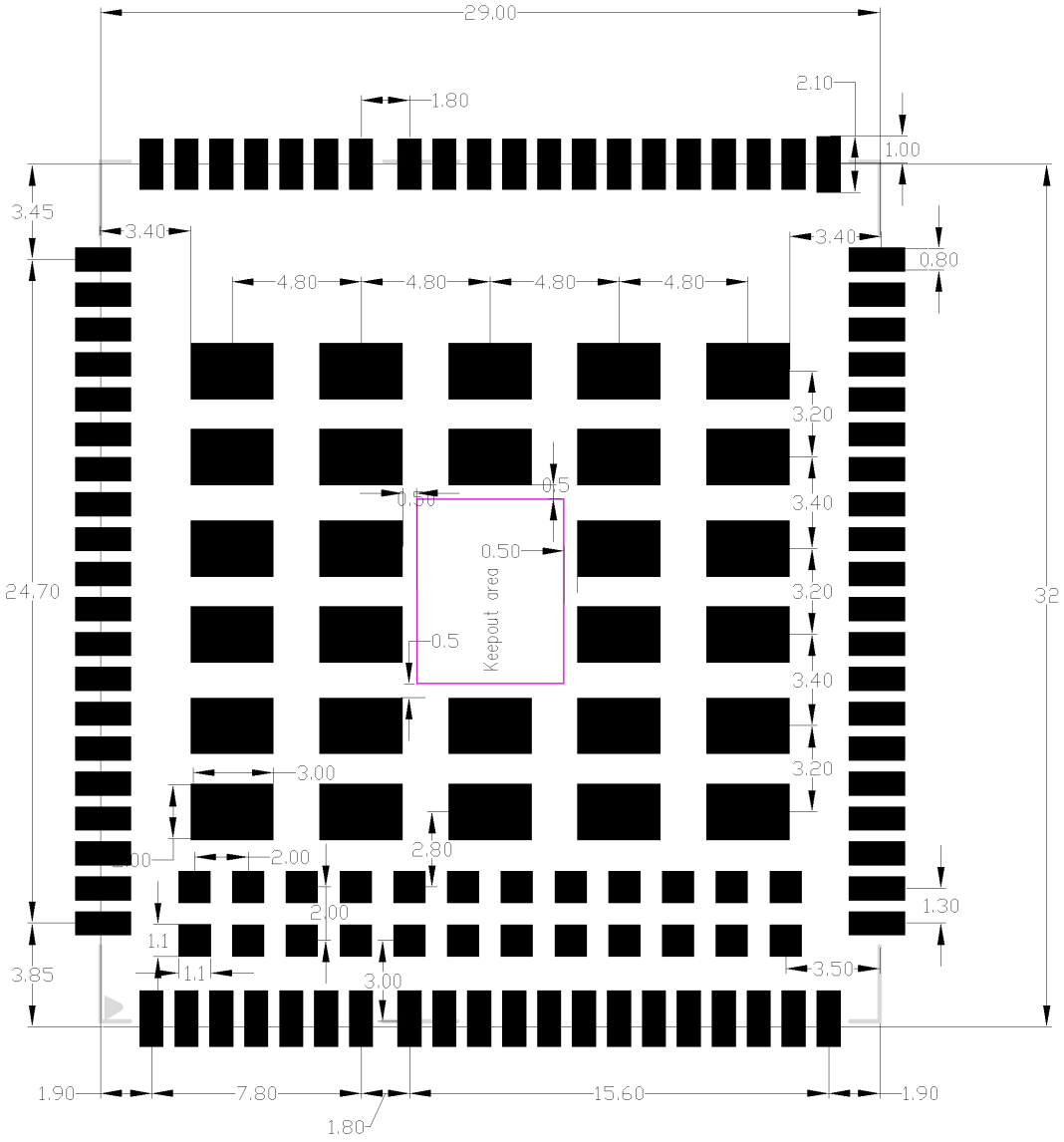

Figure 6-4 Recommended module package (unit: mm)

Chapter 7. Packaging and Production

7.1 Chapter overview

- ✧ Module packaging and storage
- ✧ Production welding

7.2 Module packaging and storage

The CLM920 AC3 module is packaged in a tray and packaged in a vacuum-sealed bag, with a 10PCS package and a 100PCS package, shipped as a vacuum-sealed bag.

The storage of the CLM920 AC3 module module is subject to the following conditions:

- ✧ The module has a moisture sensitivity rating of 3.
- ✧ When the ambient temperature is greater than 40 degrees Celsius and the air humidity is less than 90%, the module can be stored in a vacuum sealed bag for 12 months.
- ✧ When the vacuum sealed bag is opened, if the ambient temperature of the module is lower than 30 degrees Celsius and the air humidity is less than 60%, the factory can complete the patch within 72 hours, and the module can directly perform reflow soldering or other high temperature process.
- ✧ If the module is in other conditions, it needs to be baked before the patch.
- ✧ If the module needs to be baked, please remove the module and bake it for 8 hours at 125 degrees Celsius (allowing fluctuations of up to 5 degrees Celsius).

7.3 Production welding

The CLM920 AC3 module is packaged in an anti-static tray. The SMT line body needs to be equipped with a Tray module. It is recommended to use a reflow oven above 7 temperature zones.

- ✧ To ensure the quality of the module paste, the thickness of the stencil corresponding to the pad portion of the CLM920 AC3 module is recommended to be 0.18 mm.
- ✧ The recommended reflow temperature is 235~245oC, which cannot exceed 260oC.
- ✧ When the PCB is laid out on both sides, the LGA module layout must be machined on the second side. Avoid module falling parts, welding and welding, and poor internal welding of the module caused by the gravity of the module.

The recommended furnace temperature curve is shown below:

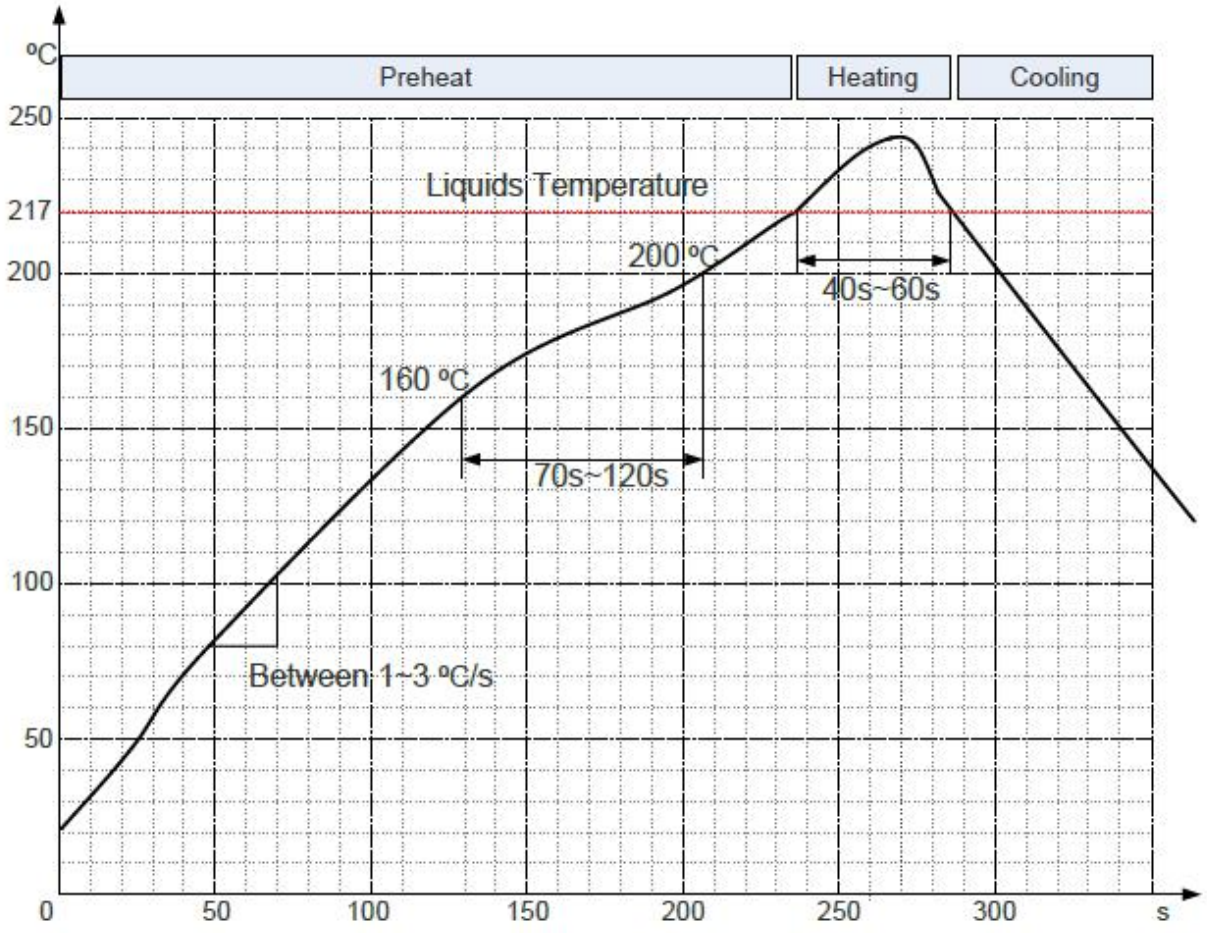

Figure 7-1 Reflow soldering temperature graph

Table 7-1 Reflow process parameter table

Warm zone	time	key parameter
Preheating zone(40℃～165℃)		Heating rate：1℃/s～3℃/s
Temperature zone(160℃～210℃)	(t1～t2)：70s～120s	
Recirculation zone(>217℃)	(t3～t4)：40s～60s	Peak temperature：235℃～245℃
Cooling zone	Cooling rate：2℃/s≤Slope≤5℃/s	

Chapter 8. Appendix

8.1 Chapter overview

- ✧ Abbreviations
- ✧ Encoding
- ✧ Safety and precautions

8.2 Abbreviations

Table 8-1 Abbreviations

Abbreviations	Full name
3GPP	Third Generation Partnership Project
AP	Access Point
AMR	Adaptive Multi-rate
BER	Bit Error Rate
CCC	China Compulsory Certification
CDMA	Code Division Multiple Access
CE	European Conformity
CSD	Circuit Switched Data
CTS	Clear to Send
DC	Direct Current
DTR	Data Terminal Ready
DL	Down Link
DTE	Data Terminal Equipment
EU	European Union
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
HSDPA	High-Speed Downlink Packet Access
HSPA	Enhanced High Speed Packet Access
HSUPA	High Speed Up-link Packet Access
IMEI	International Mobile Equipment Identity

LED	Light-Emitting Diode
LTE	Long Term Evolution
NC	Not Connected
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PMU	Power Management Unit
PPP	Point-to-point protocol
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RoHS	Restriction of the Use of Certain Hazardous Substances
SMS	Short Message Service
TIS	Total Isotropic Sensitivity
TVS	Transient Voltage Suppressor
TX	Transmitting Direction
UART	Universal Asynchronous Receiver-Transmitter
UMTS	Universal Mobile Telecommunications System
USIM	Universal Subscriber Identity Module
USSD	Unstructured Supplementary Service Data
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WWAN	Wireless Wide Area Network

8.3 Encoding

Table 8-2 Maximum HSDPA rate

HSDPA device category	Max data rate(peak)	Modulation type
Category 1	1.2Mbps	16QAM,QPSK
Category 2	1.2Mbps	16QAM,QPSK
Category 3	1.8Mbps	16QAM,QPSK
Category 4	1.8Mbps	16QAM,QPSK
Category 5	3.6Mbps	16QAM,QPSK

Category 6	3.6Mbps	16QAM,QPSK
Category 7	7.2Mbps	16QAM,QPSK
Category 8	7.2Mbps	16QAM,QPSK
Category 9	10.2Mbps	16QAM,QPSK
Category 10	14.4Mbps	16QAM,QPSK
Category 11	0.9Mbps	QPSK
Category 12	1.8Mbps	QPSK
Category 13	17.6Mbps	64QAM
Category 14	21.1Mbps	64QAM
Category 15	23.4Mbps	16QAM
Category 16	28Mbps	16QAM
Category 17	23.4Mbps	64QAM
Category 18	28Mbps	64QAM
Category 19	35.5Mbps	64QAM
Category 20	42Mbps	64QAM
Category 21	23.4Mbps	16QAM
Category 22	28Mbps	16QAM
Category 23	35.5Mbps	64QAM
Category 24	42.2Mbps	64QAM

Table 8-3 Maximum HSUPA rate

HSUPA device category	Max data rate(peak)	Modulation type
Category 1	0.96Mbps	QPSK
Category 2	1.92Mbps	QPSK
Category 3	1.92Mbps	QPSK
Category 4	3.84Mbps	QPSK
Category 5	3.84Mbps	QPSK
Category 6	5.76Mbps	QPSK

Table 8-4 LTE-FDD DL maximum rate

LTE-FDD device category	Max data rate(peak)	Modulation type
Category 1	10Mbps	QPSK/16QAM/64QAM

Category 2	50Mbps	QPSK/16QAM/64QAM
Category 3	100Mbps	QPSK/16QAM/64QAM
Category 4	150Mbps	QPSK/16QAM/64QAM

Table 8-5 LTE-FDD UL maximum rate

LTE-FDD device category	Max data rate(peak)	Modulation type
Category 1	5Mbps	QPSK/16QAM
Category 2	25Mbps	QPSK/16QAM
Category 3	50Mbps	QPSK/16QAM
Category 4	50Mbps	QPSK/16QAM

8.4 Safety and precautions

In order to use the wireless device safely, please inform the user about the safety information.:

- ✧ Interference: When the use of wireless devices is prohibited or the use of the device causes interference and security of the electronic device, turn off the wireless device. Because the terminal will send and receive RF signals when it is powered on. It can interfere with TV, radio, computer or other electrical equipment.
- ✧ Medical equipment: In medical and health care facilities where the use of wireless devices is prohibited by express text, please follow the regulations of the site and turn off the device. Some wireless devices may interfere with the medical device, causing the medical device to malfunction or cause errors. If interference occurs, turn off the wireless device and consult a physician.
- ✧ Flammable and explosive areas: In flammable and explosive areas, please turn off your wireless device and follow the relevant label instructions to avoid an explosion or fire. Such as: gas stations, fuel zones, chemical products areas and chemical transportation and storage facilities, areas with explosion hazard signs, areas with "turn off radio equipment" signs.
- ✧ Traffic Safety: Please comply with local laws or regulations in your country or region regarding the use of wireless devices when driving a vehicle.
- ✧ Aviation Safety: When flying, please follow the airline's regulations and regulations regarding the use of wireless equipment. Before taking off, turn off the wireless device to prevent wireless signals from interfering with aircraft control signals.
- ✧ Environmental Protection: Please comply with local laws regarding the handling of

equipment packaging materials, equipment or accessories, and support recycling operations.

- ✧ Emergency call: This device uses wireless signals for propagation. Therefore, the network cannot be connected in all cases, so in the emergency, the wireless device cannot be used as the only contact method.