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LPM2100 qg
NB module hardware manual

V1.0

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Chapter 1. Introduction

This document is the wireless solution product LPM2100 qg module hardware interface manual. It is intended to describe the hardware composition and functional characteristics of the module solution product, application interface definition and usage, electrical and mechanical characteristics, etc.,.Combined with this document and other application documents, users can quickly use the module to design wireless products.

Chapter 2. Product Overview

2.1 Product Overview

The LPM2100 qg module is a eMTC/NB-IOT based wireless communication module for the Internet of things. It is encapsulated for LGA with 102 pins, and the structure size of the module is 22.5mm*26.5mm*2.4mm. Support the following frequency bands:

- ✧ NB-IOT:Band1,Band3,Band4,Band5,Band8,Band18,Band19,Band20,Band26,Band28；
- ✧ eMTC: Band5、Band8@LTE-FDD/Band39@LTE-TDD;

LPM2100 qg Integrated multi constellation GNSS receiver,support GPS/GLONASS/BeiDou/Galileo/QZSS positioning system.GNSS supports at least 44 channels; tracking sensitivity can reach -153dBm;

The LPM2100 qg module uses low power technology, and the current power consumption can be as low as 5uA at deep sleep.

The LPM2100 qg module can be used in the following applications:

- ✧ Vehicle equipment
- ✧ Smart city (intelligent parking, water / gas meter, street lamp, smoke alarm, garbage bin, etc.)
- ✧ Intelligent medical treatment
- ✧ ndustrial and agricultural intelligent monitoring (machine alarm, gas detection, irrigation, soil pH value, etc.)
- ✧ Smart home
- ✧ Other wireless terminals

2.2 Module Features

Table 2-1 Module specifications

Features	description
Physical properties	22.5mm*26.5mm*2.4mm
Application processor	Single-core ARM Cortex-A7 processor, clocked at 1.2GHZ, 256kB ,level 2 cache
Working voltage	3.3V - 4.2V Typical voltage 3.7V
Power saving	PSM mode power < 5uA
Power saving	Dormant mode current < 1mA

Application interface	standard SIM interface, support 3.0V / 1.8V, support hot-swapping function USB2.0 (High-Speed) Hardware reset interface UART serial interface PCM interface power interface Network status indication interface GPIO interface
Operating frequency band	NB-IOT:Band1,Band3,Band4,Band5,Band8,Band18,Band19,Band20,Band26,Band28 eMTC: Band5、Band8@LTE-FDD/Band39@LTE-TDD;
Emissive power	LTE Power grade 3 (0.25W) E1 (0.4W)
Data service	LTE CatM1 support 1.4MHz LTE CatNB1 support 200KHz LTE CatM1 ： 375Kbps (DL) LTE CatM1 ： 375Kbps (UL) LTE CatNB1 ： 32Kbps (DL) LTE CatNB1 ： 72Kbps (UL)
Satellite positioning	GPS/BeiDou/GLONASS Protocol：NMEA
GNSS Interface	GSM/LTE Main antenna interface GNSS Antenna interface
SMS business	Support Text and PDU patterns Support point - to - point MO and MT SMS storage: USIM card /ME (default)
Operating temperature	normal working temperature －30° C to +75° C Extreme working temperature －40° C to +80° C Storage temperature:-45° C to +85° C
AT command	Supports standard AT command（Hayes 3GPP TS 27.007 和 27.005）

The LPM2100 qg module recommends working at - 30 degree C to +75 degree C environment. It is suggested that the application terminal adopt temperature control measures under harsh conditions. At the same time, some RF indexes may exceed the limit. At the same time, it is suggested to be stored under a certain temperature.

The LPM2100 qg module can further reduce its power consumption by way of entering PSM. PSM is similar to shutdown, but modules are still registered on the network. After waking from the PSM mode, the module does not need to re attach or re establish the PDN connection. So the module can not respond to user request immediately after entering PSM. The PSM function can be used by AT+CPSMS=1. In the PSM state, the module can be wake-up by pulling the PWRKEY pin to a low level.

2.3 Module Function

LPM2100 qg module contains the following circuit elements:

- ✧ Baseband processing unit
- ✧ Power management unit
- ✧ Memory unit
- ✧ RF transceiver unit
- ✧ RF front-end unit
- ✧ GPS RF receiving unit

LPM2100 qg module function block diagram is as follows:

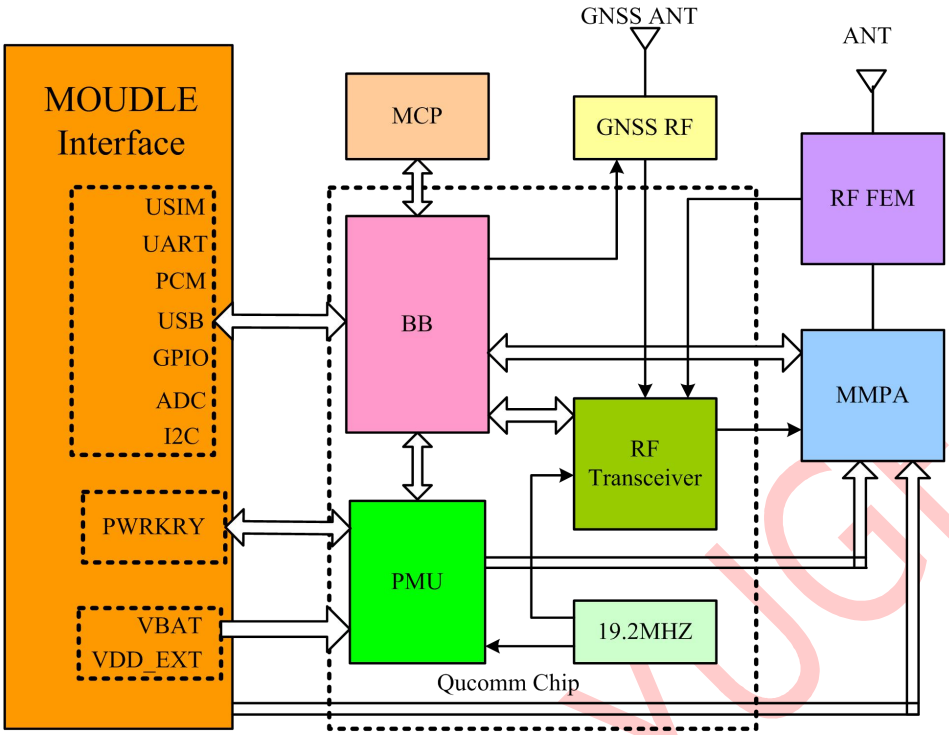

Figure 2-1 LPM2100 qg module functional block diagram

2.4 Module working mode

Table 2-2 mode of work

Working mode	Description
Turn off the machine	In the case of shutdown, the module can't work
Flight Mode	The module closes the module RF circuit, unable to interact with the network.
Dormancy	The module closes most functions, and it will synchronize with the network.
Free	Open the machine and register the network successfully, in the idle state
Data transmission	The module is in working state and has data interaction with the network.
PSM mode	After entering PSM mode, the module can achieve the minimum power consumption, each power supply inside the module is closed, the software except RTC is stopped

	running, and the serial port and USB can not be used.

Chapter 3. Interface application description

3.1 Overview of this chapter

There are 102 patch pins in LPM2100 qg. The following sections will explain the functions of each unit interface in detail.

- ✧ Modular foot distribution diagram
- ✧ Modular foot description
- ✧ Power interface
- ✧ USB interface
- ✧ USIM interface
- ✧ UART interface
- ✧ Network status indicator interface
- ✧ PCM interface
- ✧ RF antenna interface

3.2 Module Interface

3.2.1 LPM2100 qg tube foot distribution diagram

LPM2100 qg pins are assigned as follows:

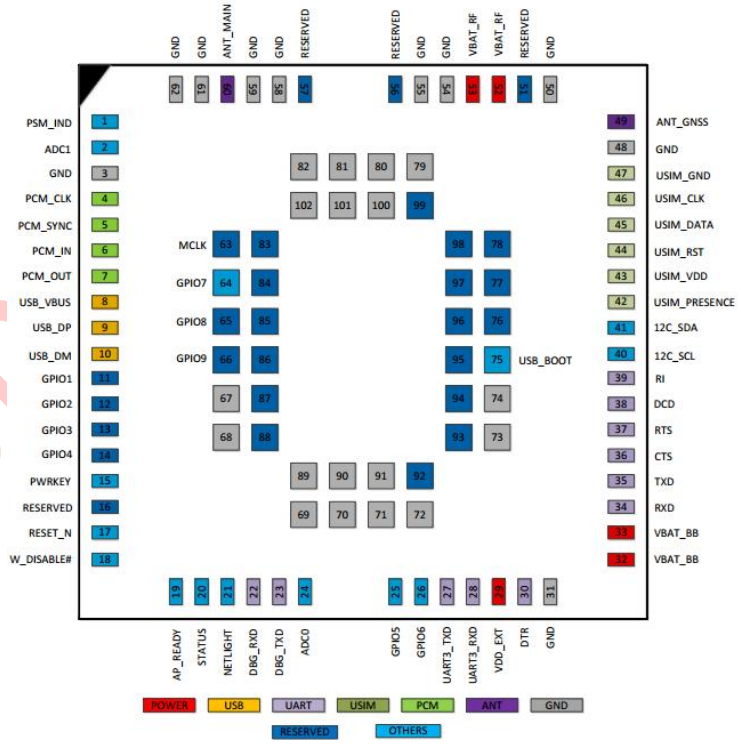

Figure 3-1 LPM2100 qg pin distribution diagram

Table 3-1 module pin definition list

Pin	Pin definition	Pin	Pin definition
1	PSM_IND	2	ADC1
3	GND	4	PCM_CLK
5	PCM_SYNC	6	PCM_IN
7	PCM_OUT	8	USB_VBUS
9	USB_DP	10	USB_DM
11	GPIO_1	12	GPIO_2
13	GPIO_3	14	GPIO_4
15	PWRKEY	16	RESERVED
17	RESET_N	18	W_DISABLE
19	AP_READY	20	STATUS
21	NETLIGHT	22	DBG_RXD
23	DBG_TXD	24	ADC0
25	GPIO_5	26	GPIO_6
27	UART3_TXD	28	UART3_RXD
29	VDD_EXT	30	DTR
31	GND	32	VBAT_BB
33	VBAT_BB	34	RXD
35	TXD	36	CTS
37	RTS	38	DCD
39	RI	40	I2C_SCL
41	I2C_SDA	42	USIM_PRESENCE
43	USIM_VDD	44	USIM_RST
45	USIM_DATA	46	USIM_CLK
47	USIM_GND	48	GND
49	ANT_GNSS	50	GND
51	RESERVED	52	VBAT_RF
53	VBAT_RF	54	GND
55	GND	56	RESERVED

57	RESERVED	58	GND
59	GND	60	ANT_MAIN
61	GND	62	GND
63	I2S_MCLK	64	GPIO_7
65	GPIO_8	66	GPIO_9
67	GND	68	GND
69	GND	70	GND
71	GND	72	GND
73	GND	74	GND
75	USB_BOOT	76	RESERVED
77	RESERVED	78	RESERVED
79	GND	80	GND
81	GND	82	GND
83	RESERVED	84	RESERVED
85	RESERVED	86	RESERVED
87	RESERVED	88	RESERVED
89	GND	90	GND
91	GND	92	RESERVED
93	RESERVED	94	RESERVED
95	RESERVED	96	RESERVED
97	RESERVED	98	RESERVED
99	RESERVED	100	GND
101	GND	102	GND

NOTE

① The module general IO port level is 1.8V (in addition to SIM, the SIM card port level support 1.8V and 3.0V).

② The module definition RESERVED and NC pins floating, shall not be used.

3.2.2. Module pin description

The definition of the module interface pipe foot is described as follows:

Table 3-2 pin parameter abbreviations

Sign indicator	Description
IO	Input or output
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
DI	Digital input
DO	Digital output
PU	Pull up
PD	Drop-down

Table 3-3 interface definition

Pin	definition	IO	Functional description	Remarks
Power supply				
32,33	VBAT_BB	PI	Baseband power supply	Input voltage3.3~4.2V
52,53	VBAT_RF	PI	Radio frequency power supply	Input voltage3.3~4.2V
29	VDD_EXT	PO	Internal 1.8V power output	Maximum current 50mA
System control				
15	PWRKEY	DI	Switch control input, low level effective	Default high level 0.8V
17	RESET_N	DI	Hardware reset control, low level effective	Far away from the source of interference
USB interface				
8	USB_VBUS	PI	USB insertion detection, high level effective	
9	USB_DP	IO	USB differential signal +	
10	USB_DM	IO	USB differential signal-	

SIM interface				
42	USIM_PRESENCE	DI	SIM card hot plug detection	External demand for 10K pullup resistance
43	USIM_VDD	PO	Output power supply to SIM card	
44	USIM_RST	DO	SIM card reset output	
45	USIM_DATA	IO	SIM card bus data	Internal 100K resistance pull up
46	USIM_CLK	DO	SIM card clock output	
47	USIM_GND			
State indication				
20	STATUS	DO	Module status indication (in development)	1.8V voltage domain
21	NETLIGHT	DO	Network status indication (in development)	1.8V voltage domain
UART1 interface				
34	RXD	DI	Data reception	1.8V voltage domain
35	TXD	DO	Data transmission	1.8V voltage domain
36	CTS	DO	Scavenging sending	1.8V voltage domain
37	RTS	DI	Request to send	1.8V voltage domain
38	DCD	DOH	Output carrier detection	Unused, suspension treatment
39	RI	DOH	Ringing indication	Unused, suspension treatment
30	DTR	DI	Data terminal preparation	Unused, suspension treatment
UART2 interface				
22	DBG_RXD	DI	Data reception	Debug UART
23	DBG_TXD	DO	Data transmission	Debug UART
UART3 serial port				
27	UART3_TX	DO	Data transmission	1.8V voltage domain

	D			
28	UART3_RXD	DI	Data reception	1.8V voltage domain
I2C interface				
40	I2C_SCL	OD	I2C bus clock output	Internal 10K resistance pull up
41	I2C_SDA	IO	I2C bus data input and output	Internal 10K resistance pull up
PCM interface				
4	PCM_CLK	DO	PCM bus data output	1.8V voltage domain
5	PCM_SYNC	DO	PCM bus synchronous output	1.8V voltage domain
6	PCM_IN	DI	PCM bus data input	1.8V voltage domain
7	PCM_OUT	DO	PCM bus data output	1.8V voltage domain
Other functional feet				
1	PSM_IND	DO	PSM status indication	1.8V voltage domain
18	W_DISABLE	DI	Flight mode control	1.8V voltage domain
19	AP_READY	DI	Detection of AP dormancy state	1.8V voltage domain
2	ADC1	AI	General analog digital converter interface	Range 0.1V~1.7V
24	ADC0	AI	General analog digital converter interface	Range 0.1V~1.7V
Universal input-output interface				
11	GPIO_1	IO	General input / output port	Reusable SPI_MOSI
12	GPIO_2	IO	General input / output port	Reusable SPI_MISO
13	GPIO_3	IO	General input / output port	Reusable SPI_CS_N
14	GPIO_4	IO	General input / output port	Reusable SPI_CLK
25	GPIO_5	IO	General input / output port	Reusable I2C_SDA
26	GPIO_6	IO	General input / output port	Reusable I2C_SCL
64	GPIO_7	IO	General input / output port	
65	GPIO_8	IO	General input / output port	

66	GPIO_9	IO	General input / output port	
Antenna interface				
49	ANT_GNSS	AI	GNSS antenna interface	
60	ANT_MAIN	IO	Main antenna interface	

3.3 Power Interface

LPM2100 qg module power interface consists of three parts:

✧ VBAT_BB/RF for the module power supply; VBAT_BB pins are used for baseband power supply, and VBAT_RF is used for RF power supply.

✧ USIM_VDD power supply for SIM card operation;

✧ VDD_EXT for internal 1.8V output power, the maximum supply of 50mA current;

3.3.1 Power supply design

LPM2100 qg module power interface is as follows:

Table 3-4 definition of power pipe feet

pins	Name	I/O	Description	Min	Typical	Max
32,33	VBAT_BB	PI	Baseband power supply	3.3V	3.7V	4.2V
52,53	VBAT_RF	PI	Radio frequency power supply	3.3V	3.7V	4.2V
43	USIM_VDD	PO	SIM power Supply	0	1.8V/ 2.85V	1.98/ 3.3V
29	VDD_EXT	PO	Output power supply		1.8V	
3,31,48,50,54, 55,58,59,61,62 ,67-74,79-82,8 9-91,100-102	GND		Ground	-	0	-

The LPM2100 qgqg module can be powered by a single power supply mode. The module has 4 channels of power supply, two VBAT_BB pins supply the baseband of the module, two VBAT_RF pins give the module radio frequency power supply, the module power supply range is between 3.3V - 4.2V, and the power supply current is not less than 2A. Because in the EGPRS network, when the instantaneous high power transmission is instantaneous, the maximum 2A

current peak will be generated, which leads to a larger ripple in the power supply. If the instantaneous voltage drop causes the VBAT power supply voltage to be too low or the power supply current is insufficient, the module may turn off or restart. Therefore, the module power supply needs to provide enough current to ensure the normal operation of the module.

When the external power supply is connected to the module, the VBAT_BB and VBAT_RF need to use the star line. The VBAT_BB line width should not be less than 1mm, and the VBAT_RF line width should not be less than 2mm. In principle, the longer the VBAT is walking, the wider the line is.

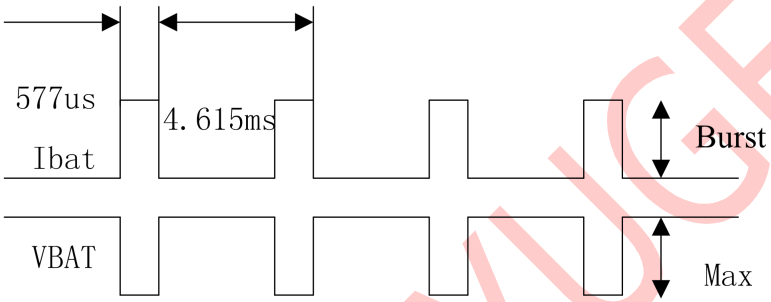

Figure 3-2 voltage drop of burst current power supply for TDMA network

In order to ensure that the power supply is sufficient, 2 470uF/6.3V tantalum capacitors can be connected in close proximity to the power input, and then a 10pF, 33pF, 0.1uF, 1uF ceramic capacitor can be added to improve the performance and stability of the system.

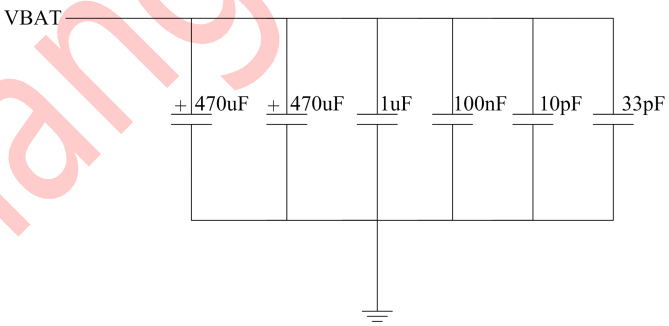

Figure 3-3 VBAT power supply power supply

3.3.2 Power reference circuit

The actual design of power supply circuit can use switched DC power supply or linear LDO power supply to design VBAT power supply, both design circuits need to provide sufficient current. Specific reference to the following circuit design:

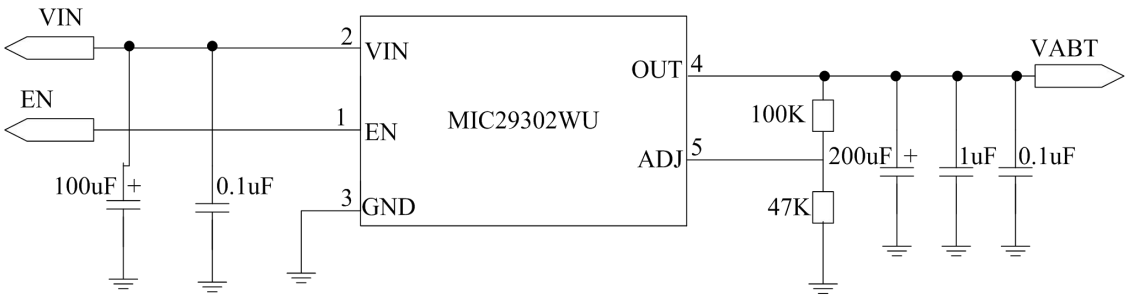

Figure 3-4 LDO linear power reference circuit

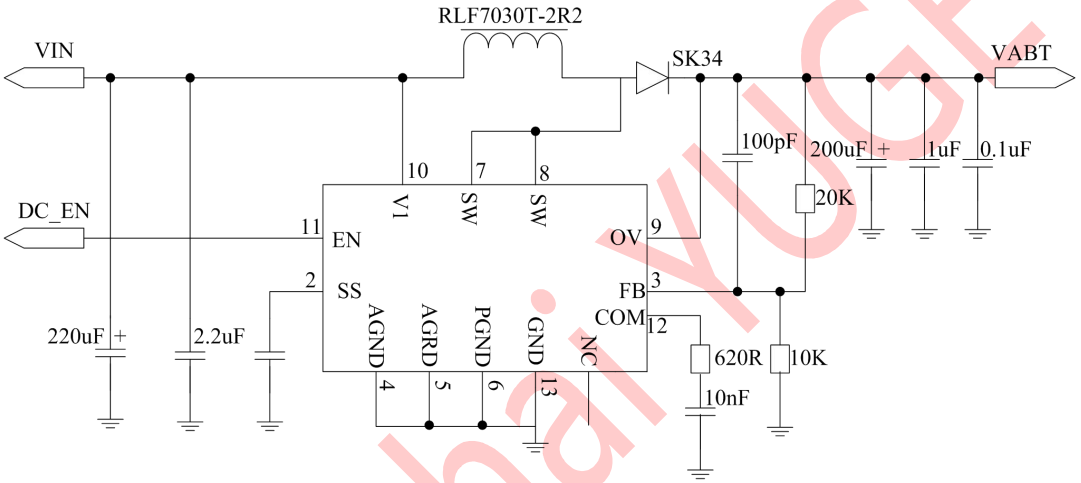

Figure 3-5 reference circuit for switching power supply

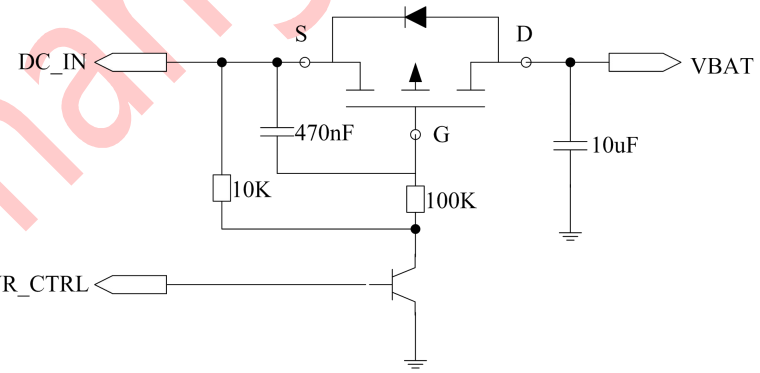

Figure 3-6 reference circuit for PMOS tube control power switch

NOTE

① In order to prevent the module from being damaged by surge and overvoltage, a 5.1V/500mW Zener diode is suggested to be connected in parallel at the VBAT pin of the module.

② It is suggested that 3 ceramic capacitors (33pF, 10pF, 100nF) be added to the VBAT pin and placed near the VBAT pin.

3.3.3 VDD_EXT 1V8 voltage output

After the LPM2100 qg module is opened normally, the twenty-ninth pins will output the voltage 1.8V, the current load is maximum 50mA. VDD_EXT can also be used as an external power supply, such as level conversion chips.

3.4 Turn on / turn off / reset

Table 3-- 5 definition of reset pin

Pin	Signal name	I/O	High value	Description
15	PWRKEY	PI	VBAT-0.3V	Low level open
17	RESET_N	DI	1.8V	Module reset control foot, low efficiency

3.4.1.Module opening

In the case of power supply, there are three kinds of modules: 1: button. A switch key 2: grounding can be linked at PWRKEY. Control the PWRKEY directly to the ground 3:AP. The user can pull up the PWRKEY pin by at least 500mS and then pull it up to enable the module to turn on. It is suggested to use open set drive circuit to control PWRKEY pins. The AP control reference circuit is illustrated as follows:

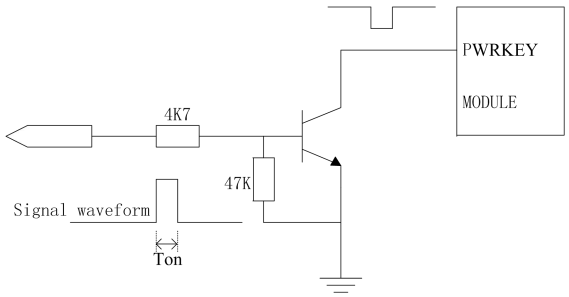

Figure 3-7 open reference circuit

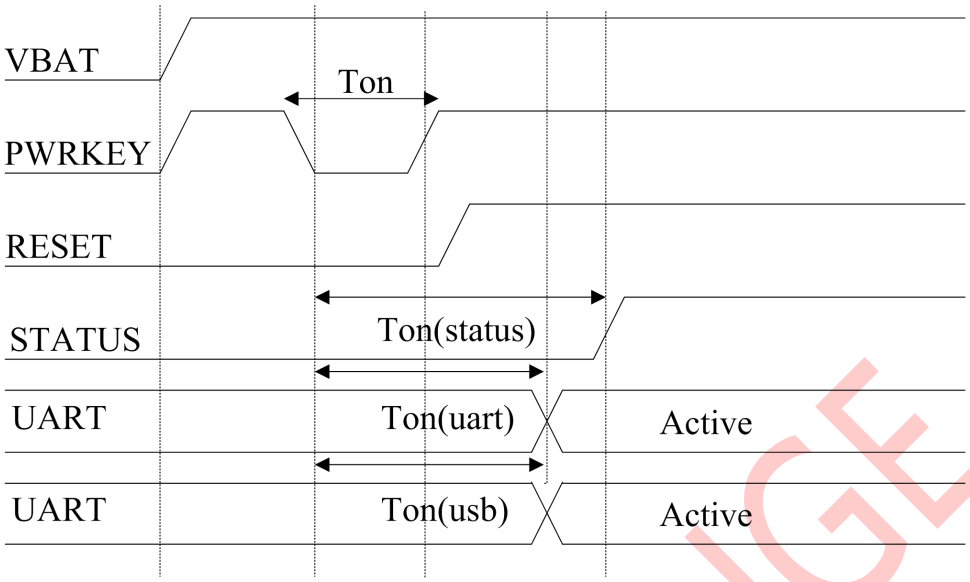

Figure 3-8 opening sequence diagram

Table 3-6 opening timing parameters

Symbol	Description	MIN	Typical	max	unit
Ton	Open low level width	100	500	-	ms
Ton(status)	Start time (according to status state)	4.5	-	-	s
Ton(usb)	Start time (according to USB state)	3.5		-	s
Ton(uart)	Start time (according to UART state)	3.5		-	s
VIH	PWRKEY input high level	0.6	0.8	1.8	V
VIL	PWRKEY input low level	-0.3	0	0.5	V

3.4.2 Module shutdown

The shutdown of LPM2100 qg module can be shutdown by PWRKEY and AT commands. The command is AT$QCPWRDN

When the module is in the boot state, the PWRKEY pin is pulled down at least 1.2S, and the module will execute the shutdown process. The shutdown sequence diagram is as follows:

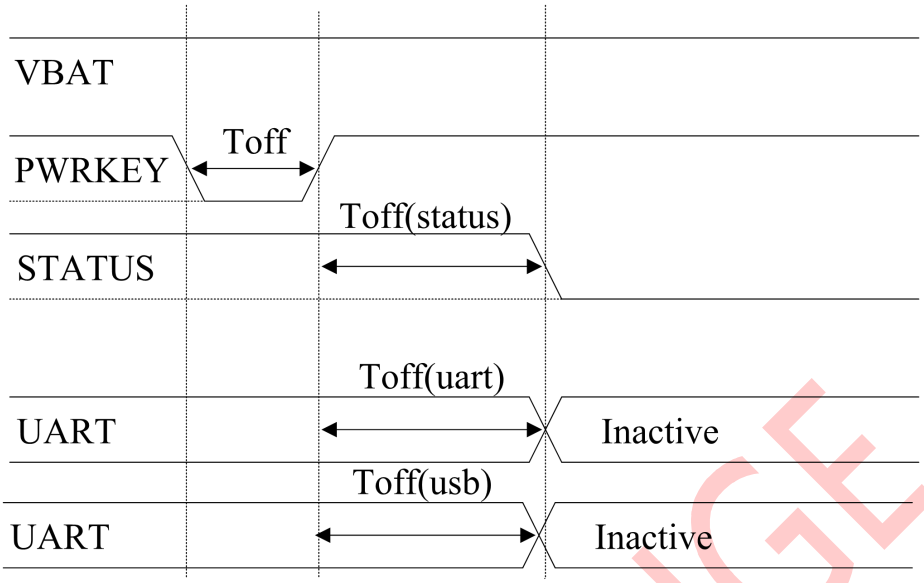

Figure 3-9 shutdown sequence diagram

Table 3-7 shutdown timing parameters

Symbol	Description	MIN	Typical	max	unit
Toff	Low level pulse width of shutdown	1.2		-	s
Toff(status)	Start time (according to status state)	2	-	-	s
Toff(usb)	Start time (according to USB state)	2		-	s
Toff(uart)	Start time (according to uart state)	2		-	s

3.4.3 Reset control

PM2100 module PIN17 signal is the RESET_N reset pin. When the application end needs to reset the module, the pin can be lowered by 100ms < Treset < 600ms and the module can be reset. The external resistance of the pin is 10K to VDD_EXT. The RESET_N pin is sensitive to interference and needs to stay away from the RF interference signal.

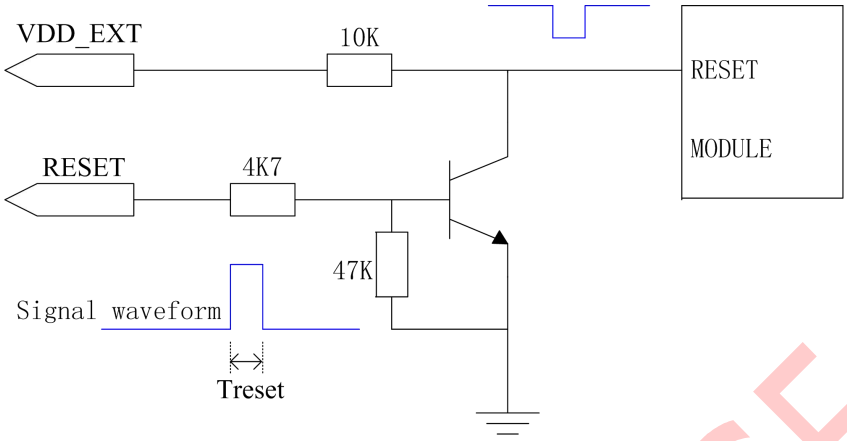

Figure 3-10 reset reference circuit

Table 3-8 RESET pin parameters

Symbol	Description	MIN	Typical	max	unit
Treset	Low level pulse width	100		600	ms
VIH	RESET input high level voltage	1.3	1.8	2.1	V
VIL	RESET input low level voltage	-0.3	0	0.5	V

LPM2100 qg module supports the AT command reset, and the AT instruction is at+cfun=1,1 to restart the module. Detailed instructions can be used to view the LPM2100 qg AT instruction set manual.

3.5 USB interface

LPM2100 qg module USB interface supports USB2.0 high-speed protocol.It can be used for software debugging, software upgrading, data transmission and AT command.Interface supports slave device mode and does not support USB charging mode.The USB interface pin is defined as follows:

Table 3-9 USB interface pipe definition

PIN	Signal name	IO	Description
8	USB_VBUS	PI	USB insertion detection, high level effective

9	USB_DP	IO	USB differential signal +
10	USB_DM	IO	USB differential signal -

Module as USB slave device, supporting USB dormancy and wakeup mechanism.The USB interface application reference circuit is as follows:

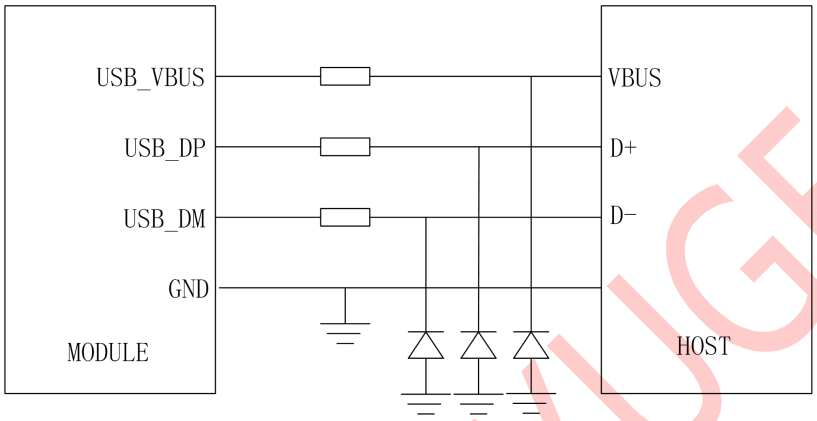

Figure 3-11 USB connection design circuit diagram

NOTE

① The USB interface supports the high speed (480Mbps) and the full speed (12Mbps) mode, so the line design needs to strictly follow the requirements of the USB2.0 protocol, pay attention to the protection of the data line, the differential walk line, and the control impedance of 90 Omega.

② In order to improve the antistatic performance of USB interface, it is suggested to add ESD protection device to the data line, and the equivalent capacitance of protection device is less than 1 pF.

③ the power supply voltage of the USB interface bus is provided by the module without external supply. At the same time, because the module's USB interface does not provide USB bus power, modules can only be used as slave devices of USB bus devices.The USB interface supports the following functions:

- ✧ Software download and upgrade
- ✧ Data communication
- ✧ AT Command
- ✧ GNSS NMEA Output

3.6 UART Interface

LPM2100 qg module provides a full function serial port for communication. The serial level is 1.8V.

The module supports three serial ports at the same time.

PIN	NAME	IO	Functional description	Remarks
34	RXD	DI	Data reception	1.8 voltage domain
35	TXD	D0	Data transmission	1.8 voltage domain
30	DTR	DI	Data terminal preparation	Unused, suspension treatment
38	DCD	DOH	Output carrier detection	Unused, suspension treatment
39	RI	DOH	Ringing indication	Unused, suspension treatment
22	DBG_RXD	DI	Data reception	1.8 voltage domain
23	DBG_TXD	DO	Data transmission	1.8 voltage domain
27	UART3_TXD	DO	Data transmission	1.8 voltage domain
28	UART3_RXD	DI	Data reception	1.8 voltage domain

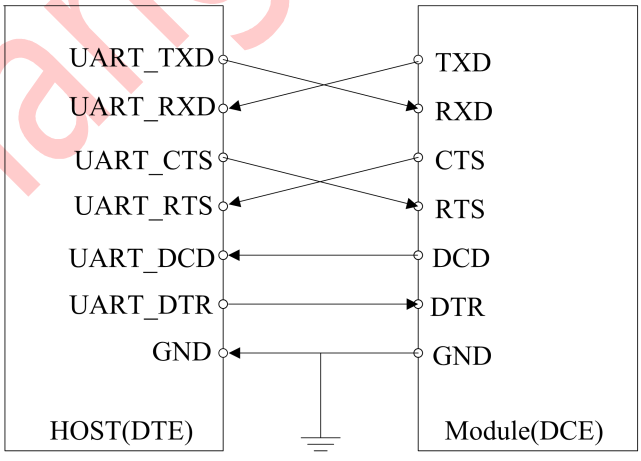

Figure 3-12 full function UART serial port design diagram

If you need to use the two wire serial port, you need to refer to the following serial port design.

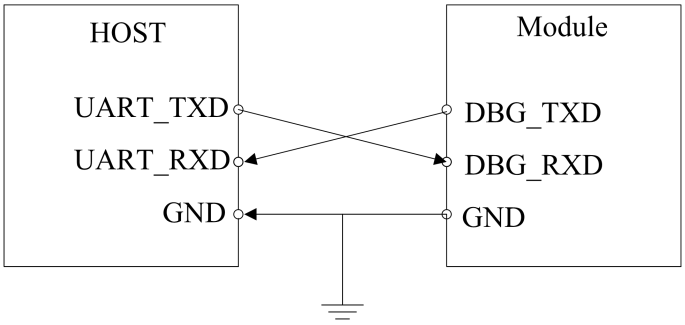

Figure 3-13 two line UART serial port design diagram

LPM2100 qg module is a TTL 1.8V level. If the serial port needs to be connected to the MCU of the 3.3V level, a level conversion chip needs to be added to achieve the level matching. The reference circuit is recommended as follows:

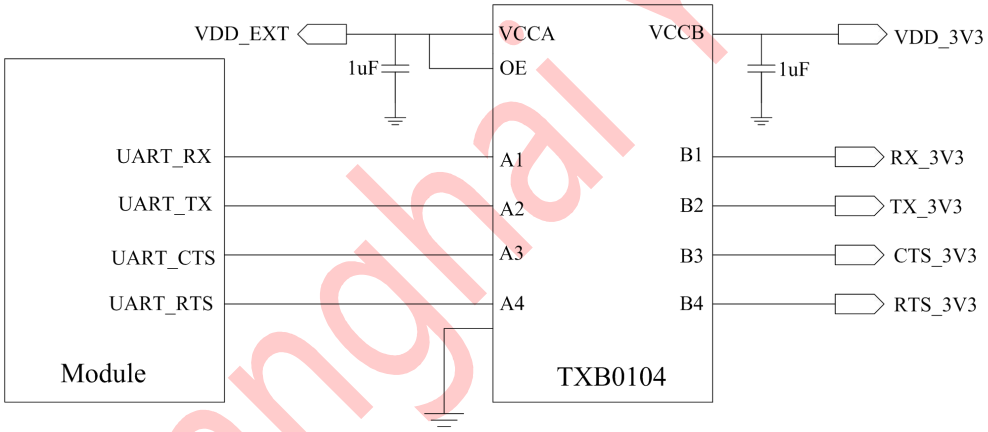

Figure 3-14 level conversion chip circuit

3.7 USIM interface

LPM2100 qg module provides a USIM card interface compatible with the ISO 7816-3 standard. The USIM card power supply is provided by the module internal power manager, and supports 1.8V/3.0V voltage.

Table 3-10 USIM card signal definition

PIN	Signal name	IO properties	High value	Description
42	USIM_PRESENCE	DI	1.8V	SIM hot-plug detection
43	USIM_VDD	PO	1.8V/2.95V	USIM card power supply

44	USIM_RST	DO	1.8V/2.95V	SIM card reset output
45	USIM_DATA	IO	1.8V/2.95V	USIM card data signal
46	USIM_CLK	DO	1.8V/2.95V	SIM card clock signal
47	USIM_GND			

3.7.1 USIM card reference circuit

LPM2100 qg module does not contain USIM card slot. Users need to design USIM card slot on their own interface board.

The USIM card interface reference circuit is as follows:

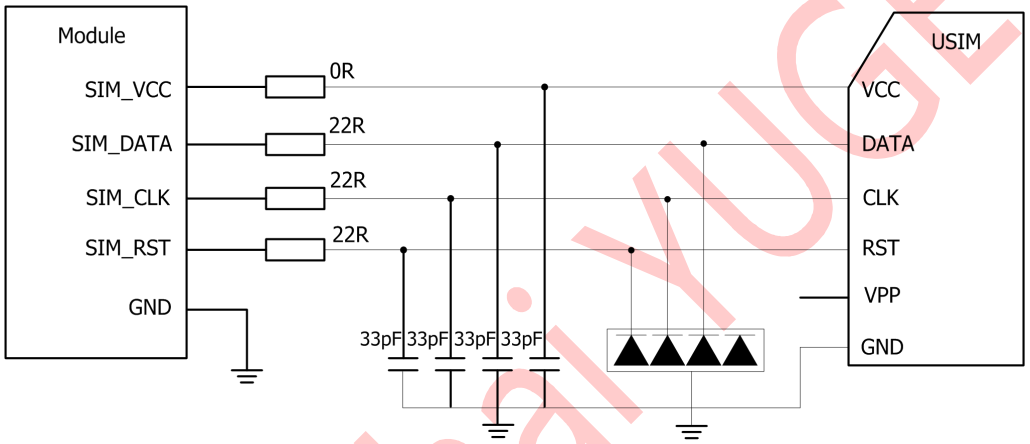

Figure 3-15 USIM design circuit diagram

NOTE

① The USIM interface line suggests choosing ONSEMI's SMF15C device to do ESD protection, and the peripheral circuit devices should be placed near the card holder. The SIM card seat is close to the module layout.

② USIM card circuit is easily caused by radio frequency interference to cause non recognition card or card loss, so the slot should be placed far away from the antenna radiofrequency radiation, the signal line is far away from the radio frequency, power and high-speed signal line.

③ The internal USIM_DATA signal has been pulled to VDD_EXT through 47K resistor, and no external pull is required.

④ USIM_PRESENCE is USIM card insert or not insert detection foot, External pull up 100K，default high level, hot-plug application can be through this pin to detect SIM card status.

⑤ To avoid transient voltage overload, USIM interface is recommended to connect 22R

resistor in series on signal path.

⑥ The ground and module of USIM card holder should maintain good connectivity.

3.7.2 USIM_PRESENCE Reference design of hot plug

LPM2100 qg module supports the hot plug detection function of USIM card.

USIM_PRESENCE pin is used as an input detection pin to determine whether the USIM card is inserted or not.pin is defaults to the high level.

Table 3-11 SIM card hot plug detection foot definition

NO	Tube foot detection state	Functional description
1	high	SIM card is inserted, UIM_DET is high
2	low	SIM card is pulled out, UIM_DET is low

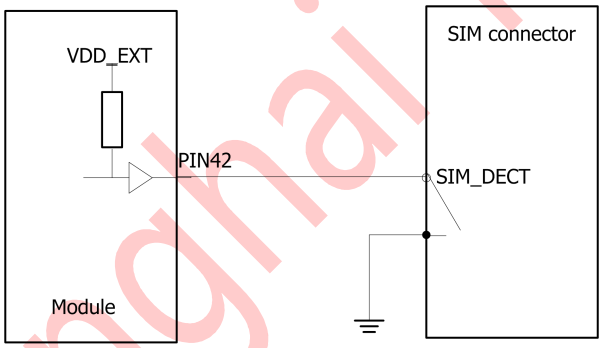

Figure 3-16 USIM card Hot pluggable detection

NOTE

① When using normally closed SIM or normally open SIM card, the detection function can be set by AT command. If AT + HOSCFG = 1.1 SIM card in place when the state is high, set AT + HOSCFG = 1,0 SIM card in place when the state is low

② The internal UIM_DATA has been pulled to VDD_EXT through 15K resistor, and no external pull is required.

3.8 PCM digital voice interface

LPM2100 qg module provides a set of PCM audio interface for external codec audio decoder chip. It supports 8 bit A rate, U rate and 16 bit linear short frame coding format, PCM_SYNC is 8kHZ and PCM_CLK is 2048kHZ.

Table 3-12 PCM pin definition

PIN	Signal name	IO properties	Description
4	PCM_CLK	D0	PCM clock pulse
5	PCM_SYNC	D0	PCM frame synchronization signal
6	PCM_IN	DI	PCM data input
7	PCM_OUT	DO	PCM data output

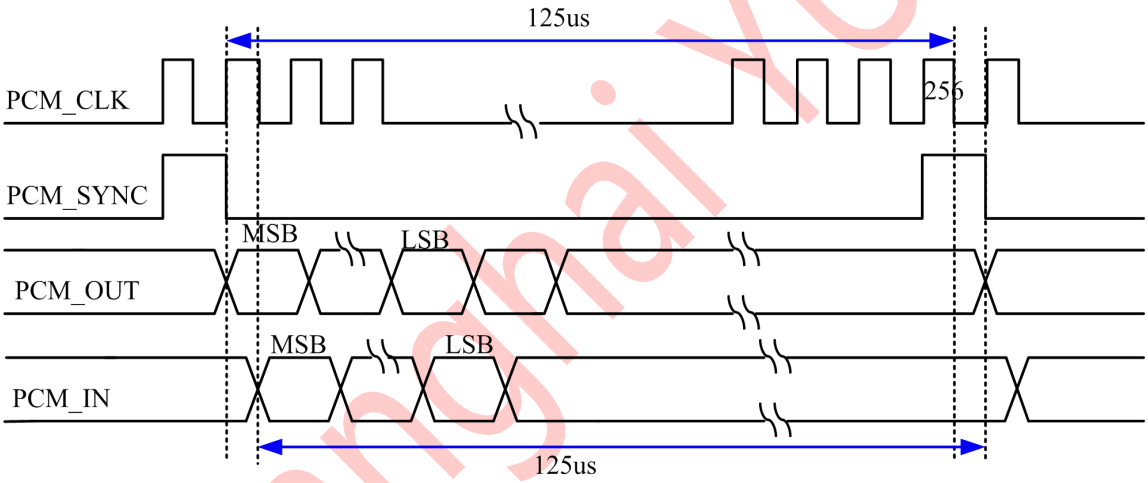

Figure3-17 PCM short frame pattern sequence diagram

3.9 Network indicator interface

LPM2100 qg module provides a NENLIGHT pin indicating the status of network communication, which can be used to drive the LED lamp indicating the network state.

Table 3-13 definition of network indicator lamp

Pin name	Pin	I/O properties	Description
NETLIGHT	21	DO	Network status indication

Table 3-14 network indicator state

State	LED display status
No service	Always on
Successful registration network	Double flash
Data transmission	Flash

LED network indicator reference design is as follows:

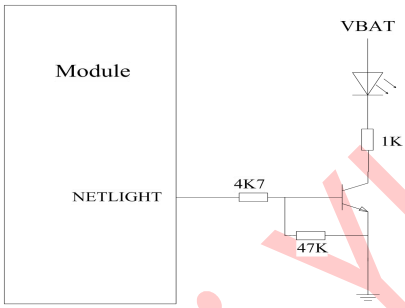

Figure 3-18network indicator circuit diagram

NOTE

The resistance value in the circuit diagram of the network indicator can be adjusted according to the LED lamp parameters.

3.10 General purpose GPIO interface

LPM2100 qg module provides multiple GPIO. Some of these GPIO can be reused as a variety of functions. The specific usage can be consulted by the module provider.

Table 3-15General Purpose GPIO Pin Definitions

Pin	Pin name	IO	Functional description	Remarks
11	GPIO_1	IO	General input / output port	Reusable SPI_MOSI
12	GPIO_2	IO	General input / output port	Reusable SPI_MOSI
13	GPIO_3	IO	General input / output port	Reusable SPI_CS_N
14	GPIO_4	IO	General input / output port	Reusable SPI_CLK
25	GPIO_5	IO	General input / output port	Reusable I2C_SDA

26	GPIO_6	IO	General input / output port	Reusable I2C_SCL
64	GPIO_7	IO	General input / output port	
65	GPIO_8	IO	General input / output port	
66	GPIO_9	IO	General input / output port	

Chapter 4. Overall technical indicators

4.1 Overview of this chapter

LPM2100 qg module radio contains the following sections:

- ✧ Operating frequency;
- ✧ Conducted RF measurements;
- ✧ Conducted receiver sensitivity and transmit power;

4.2 Operating frequency

Table 4-1 radiofrequency frequency meter

Frequency band	Uplink frequency	Downlink frequency	Duplex mode
LTE B1	1920MHz - 1980MHz	2110MHz - 2170MHz	FDD
LTE B3	1710MHz - 1785MHz	1805MHz - 1880MHz	FDD
LTE B4	1710MHz - 1755MHz	2110MHz - 2155MHz	FDD
LTE B5	824MHz – 849MHz	869MHz – 894MHz	FDD
LTE B8	880 MHz – 915 MHz	925 MHz – 960 MHz	FDD
LTE B18	815MHz - 830MHz	860MHz - 875MHz	FDD
LTE B19	830MHz - 845MHz	875MHz - 890MHz	FDD
LTE B20	832MHz - 862MHz	791MHz - 821MHz	FDD
LTE B26	814MHz - 849MHz	859MHz - 894MHz	FDD
LTE B28	703MHz - 748MHz	758MHz - 803MHz	FDD

4.3 Conducted RF Measurements radio frequency.

4.3.1 Test environment

Table 4-2 Test Instruments

test instrument	power supply		Murata coaxial RF cable
CMW500	Agilent 66319		MXHP32HP1000

4.3.2 Test standards

LPM2100 qg module passes the 3GPP TS 51.010-1, 3GPP TS 34.121-1, 3GPP TS 36.521-1, 3GPP2 C.S0011 and 3GPP2 C.S0033 test standards. Each module in the factory through rigorous

testing to ensure reliable quality.

4.4 Conducted receive sensitivity and transmit power

The test indicators of the transmission power of the LPM2100 qg module are as follows：

Table 4-3 radiofrequency indicators for conduction emission

Directories	3GPP protocol requirements (dBm)	Min
NB-IOT		
LTE B1	21 to 25	<-44dBm
LTE B3	21 to 25	<-44dBm
LTE B4	21 to 25	<-44dBm
LTE B5	21 to 25	<-44dBm
LTE B8	21 to 25	<-44dBm
LTE B18	21 to 25	<-44dBm
LTE B20	21 to 25	<-44dBm
LTE B26	21 to 25	<-44dBm
LTE B28	21 to 25	<-44dBm
eMTC		
LTE B39	21 to 25	<-44dBm
LTE B8	21 to 25	<-44dBm
LTE B5	21 to 25	<-44dBm

Table 4-4 radiofrequency sensitivity index

Directory (sensitivity)	3GPP protocol requirements	Min	Typical	max
NB-IOT				
LTE B1	-107.5	<-107.5		
LTE B3	-107.5	<-107.5		
LTE B4	-107.5	<-107.5		
LTE B5	-107.5	<-107.5		
LTE B8	-107.5	<-107.5		
LTE B18	-107.5	<-107.5		

LTE B20	-107.5	<-107.5		
LTE B26	-107.5	<-107.5		
LTE B28	-107.5	<-107.5		
eMTC				
LTE B5	-100.8	<-100.8		
LTE B8	-99.8	<-99.8		
LTE B39	-103	TBD		

4.5 Antenna requirements

LPM2100 qg module supports one main antenna and one GNSS antenna. In the design of antenna circuits, the 50 ohmic impedance is required for the alignment between modules and antennas. The RF antenna pin is defined as follows:

Table 4-5 RF pin definition

Pin	Pin name	IO	Functional description	Remarks
49	ANT_GNSS	AI		GNSS antenna interface
60	ANT_MAIN	IO		Main antenna interface

To minimize losses on the RF line or RF cable, it is recommended that insertion loss meet the following requirements:

- ✧ 880--960MHZ <0.7dB
- ✧ 1710-1920MHZ <1.2dB

When the circuit board is designed, the parameters of the matching device parameters are optimized according to the user's circuit board. Propose a reserved matching circuit.The main board R1/R2 acquieses 0 ohms and C1/C2 default. In order to prevent the internal static damage module, it is suggested to select a bidirectional TVS tube at the D1/D2 of the antenna connection.

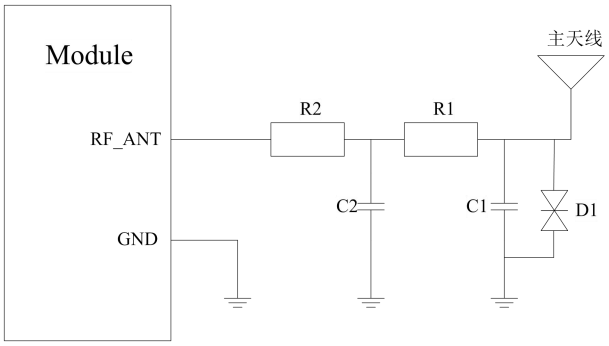

Figure 4-1 antenna connection circuit diagram

Table 4-6 GNSS antenna requirements

Frequency band	Standing wave ratio	Active antenna noise coefficient	Active antenna gain	LNA gain embedded in active antenna
GPS L1 1575.41+/1.023MHZ	<2:1	<1.5DB	>-2DBi	20DB
GLONASS 1597.5-1605.8MHZ	<2:1	<1.5DB	>-2DBi	20DB
BeiDou 1559.05-1563.14MHZ	<2:1	<1.5DB	>-2DBi	20DB

If RF connector is used for antenna connection, Murata's MM9329-2700 connector is recommended.

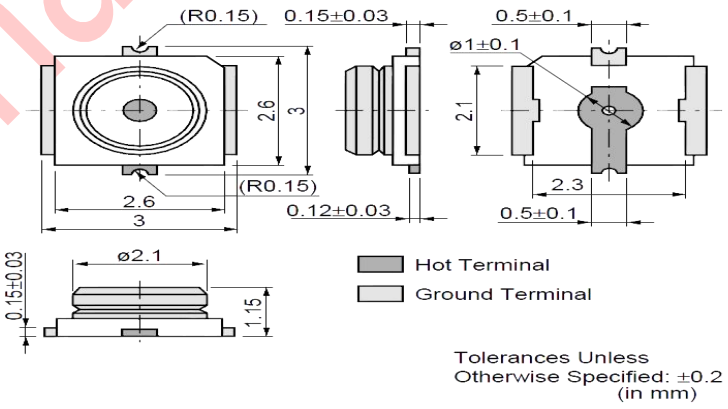

Figure 4-2 recommends a RF connector size diagram

Table 4-7 RF connector main parameters

Rated condition		environment condition
frequency range	DC to 6GHZ	－40° C to +85° C
characteristic impedance	50Ω	－40° C to +85° C

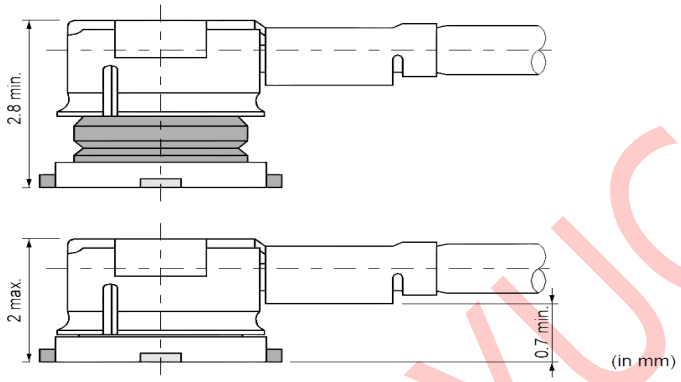

Figure 4-3 matching coaxial radio frequency line size diagram

4.6 Power consumption characteristics

Table 4-8 NB-IOT and eMTC power consumption

type	Test bandwidth	modulation mode	Call Current（mA）	
		QPSK	Avg Current	23dB Current
eMTC B5	5M			197
eMTC B8	5M			200
eMTC B39	TBD			TBD
NB-IOT B1	-			215
NB-IOT B3	-			216
NB-IOT B4	-			207
NB-IOT B5	-			210
NB-IOT B8	-		212	

NB-IOT B18	-		210
NB-IOT B20	-		219
NB-IOT B26	-		215
NB-IOT B28	-		TBD

Chapter 5. Interface electrical characteristics

5.1 Limit condition

Table 5-1 LPM2100 qg module working storage temperature

Parameter	Min	Max
normal working temperature	-30° C	80° C
Extreme working temperature	-40° C	85° C
Storage temperature:	-45° C	90° C

Table 5-2 limit operating voltage range of LPM2100 qg module

Parameter	Description	Min	Typical	Max
VBAT_BB VBAT_RF	Module power supply voltage	3.3V	3.7V	4.2V
	RMS average current			0.9V
	GSM TDMAInstantaneous pressure drop			300mV

5.2 Module IO electrical level

LPM2100 qg module IO electrical level is as follows:

Which corresponds to 1.8V USIM application, USIM_VDD is 1.8V, corresponds to 3V USIM application, USIM_VDD is 2.85V.Other digital IO levels are unified to 1.8V.

Table 5-3 electrical characteristics of LPM2100 qg module

Parameter	Description	Min	Max
VIH	High level input voltage	0.65* VDD_EXT	VDD_EXT+0.3V
VIL	Low level input voltage	-	0.35*VDD_EXT
VOH	High level output voltage	VDD_EXT-0.45V	VDD_EXT
VOL	Low-level output voltage	0	0.45V

5.3 Electrostatic characteristics

LPM2100 qg module needs to protect ESD when it is used to ensure product quality.

Table 5-4 LPM2100 qg ESD characteristics

Test port	Contact discharge	Air discharge	Unit
USB interface	±4	±8	KV
USIM interface	±4	±8	KV
VBAT power supply	±4	±8	KV

Chapter 6. Mechanical Size

This section describes the mechanical dimensions of the module.

6.1 Modular mechanical size

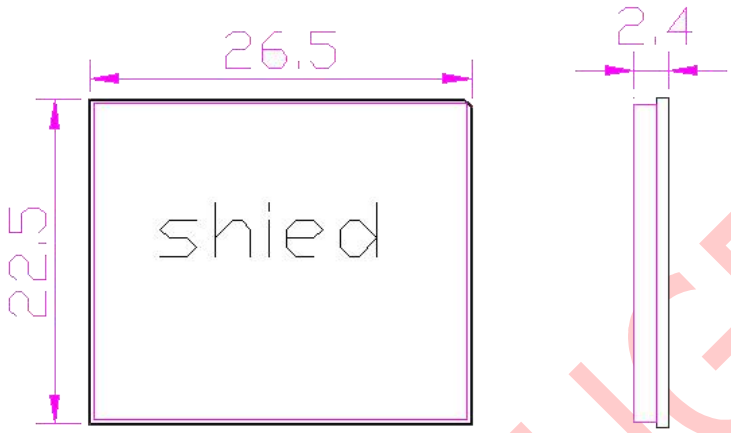

Figure 6-1 LPM2100 qg mechanical size diagram (unit mm)

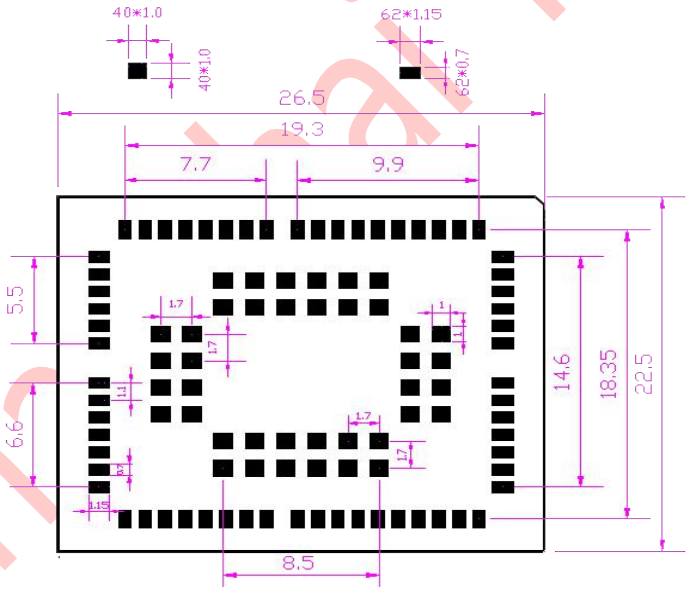

Figure 6-2 LPM2100 qg bottom dimension diagram (unit mm)

6.2 Module overlook and bottom view

The printing scraper is used to print the solder paste on the net plate, so that the solder paste is imprinted on the PCB through the opening of the net plate. The strength of the printing scraper needs to be suitable. In order to ensure the quality of the block printing paste, the thickness of the

steel net corresponding to the part of the module welding plate should be 0. 18mm.

Figure 6-3 LPM2100 qg overlook view

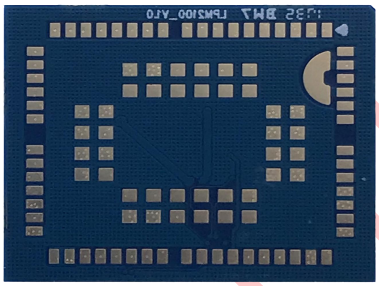

Figure 6-4 LPM2100 qg bottom view

Chapter 7. patch production

7.1 Summary

- ✧ Packaging and storage of module
- ✧ Production welding

7.2 Module packaging and storage

LPM 2100 bg NB module is packed in tray and packed in vacuum sealed bag. It is shipped in the form of vacuum sealed bag with 10PCS as a disk and 100PCS as a package.

The storage of LPM2100 qg bg NB module module should follow the following conditions:

- ✧ The humidity sensitive grade of the module is level 3.
- ✧ If the ambient temperature is greater than 40 degrees Celsius and the air humidity is less than 90%, the module can be stored in a vacuum sealed bag for 12 months.
- ✧ When the vacuum sealing bag is opened, if the temperature of the module is less than 30 degrees centigrade, the air humidity is less than 60%, the factory can finish the patch within 72 hours, and the module can be directly reflow welding or other high temperature flow.
- ✧ If the module is in other conditions, it needs baking before the patch.
- ✧ If the module needs to be baked, remove the package and bake at 125 degrees Celsius for 48 hours.

7.3 Production welding

LPM 2100 bg NB module is packed by antistatic tray, SMT production line should be equipped with Tray module, reflux furnace above 7 temperature zone is recommended.

- ✧ To ensure the quality of the printing paste, the thickness of the steel mesh corresponding to the pad of the LPM2100 qg bg NB module is recommended as 0.18mm.
- ✧ It is recommended that the temperature of reflow soldering is 235~245 C, not exceeding 260 C.
- ✧ When PCB double sided layout, LCC module layout must be processed on second sides. Avoid module reversal due to module gravity, resulting in module missing, welding and welding, and poor internal welding of modules.

The recommended temperature curve of the furnace is as shown in the following figure.

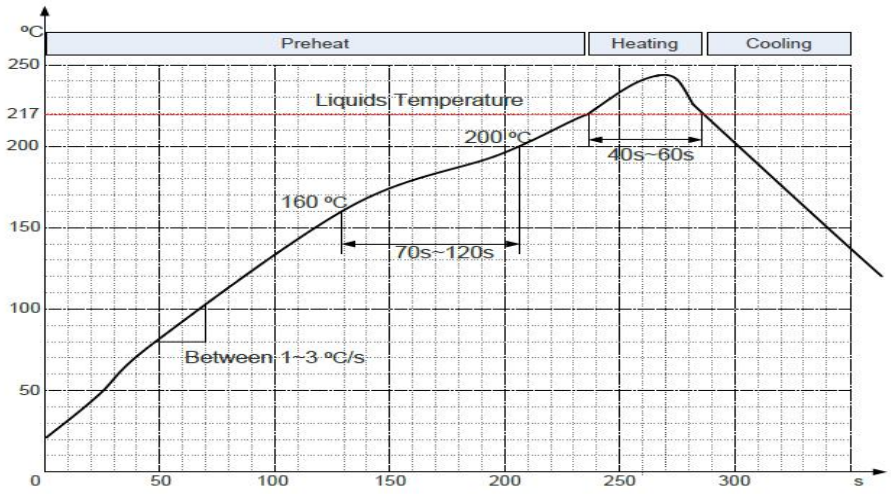

Figure 7-1 reflow soldering temperature curve

Chapter 8. Terminology abbreviation

Table 8-1 terminology abbreviations

Abbreviation	Full name
3GPP	Third Generation Partnership Project
AMR	Adaptive Multi-rate
CTS	Clear to Send
DTR	Data Terminal Ready
DL	Down Link
DTE	Data Terminal Equipment
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
LED	Light-Emitting Diode
NC	Not Connected
PCB	Printed Circuit Board
USIM	Universal Subscriber Identity Module
TVS	Transient Voltage Suppressor
TX	Transmitting Direction
UART	Universal Asynchronous Receiver-Transmitter
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
UART	Universal Asynchronous Receiver-Transmitter
USIM	Universal Subscriber Identity Module